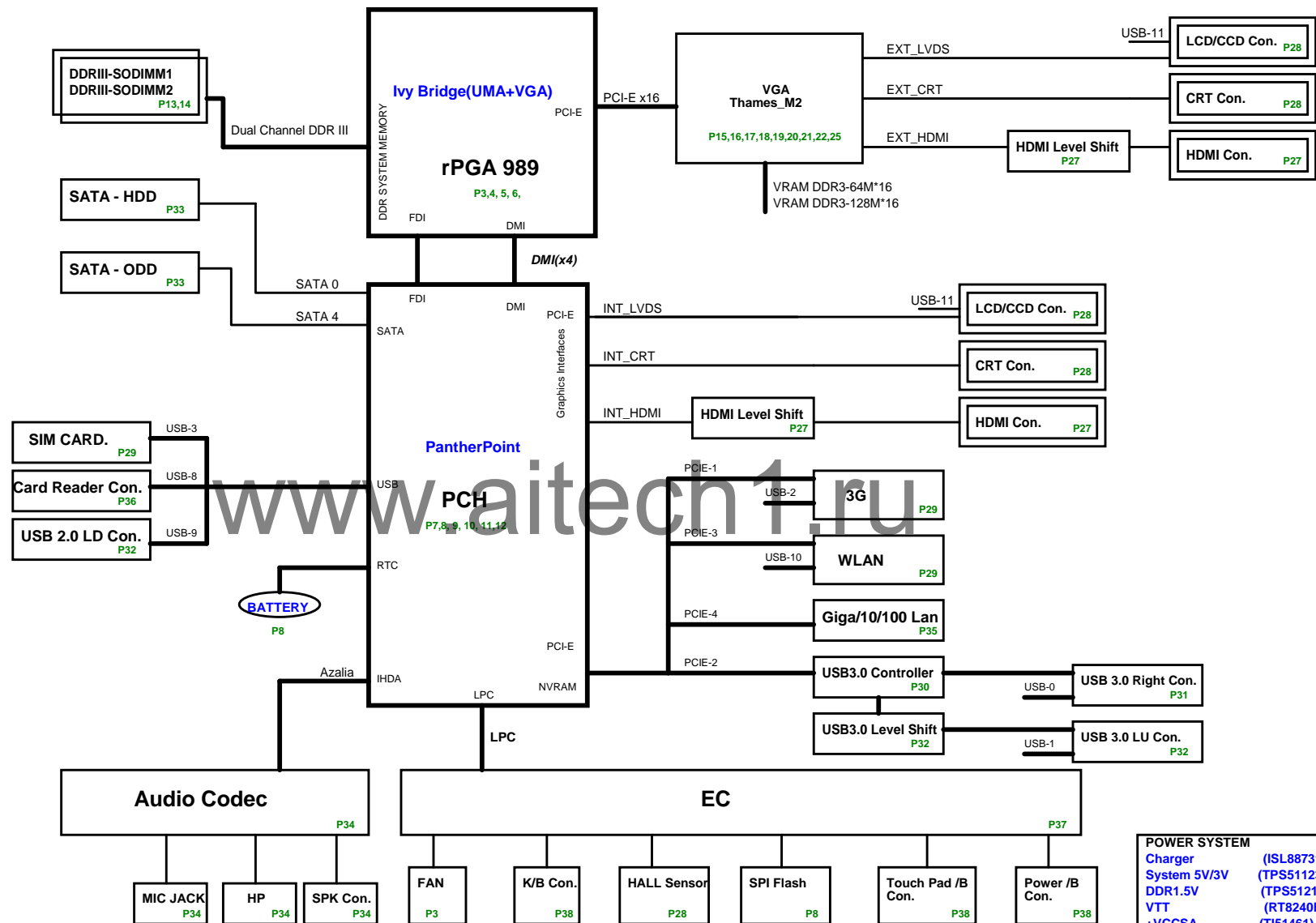
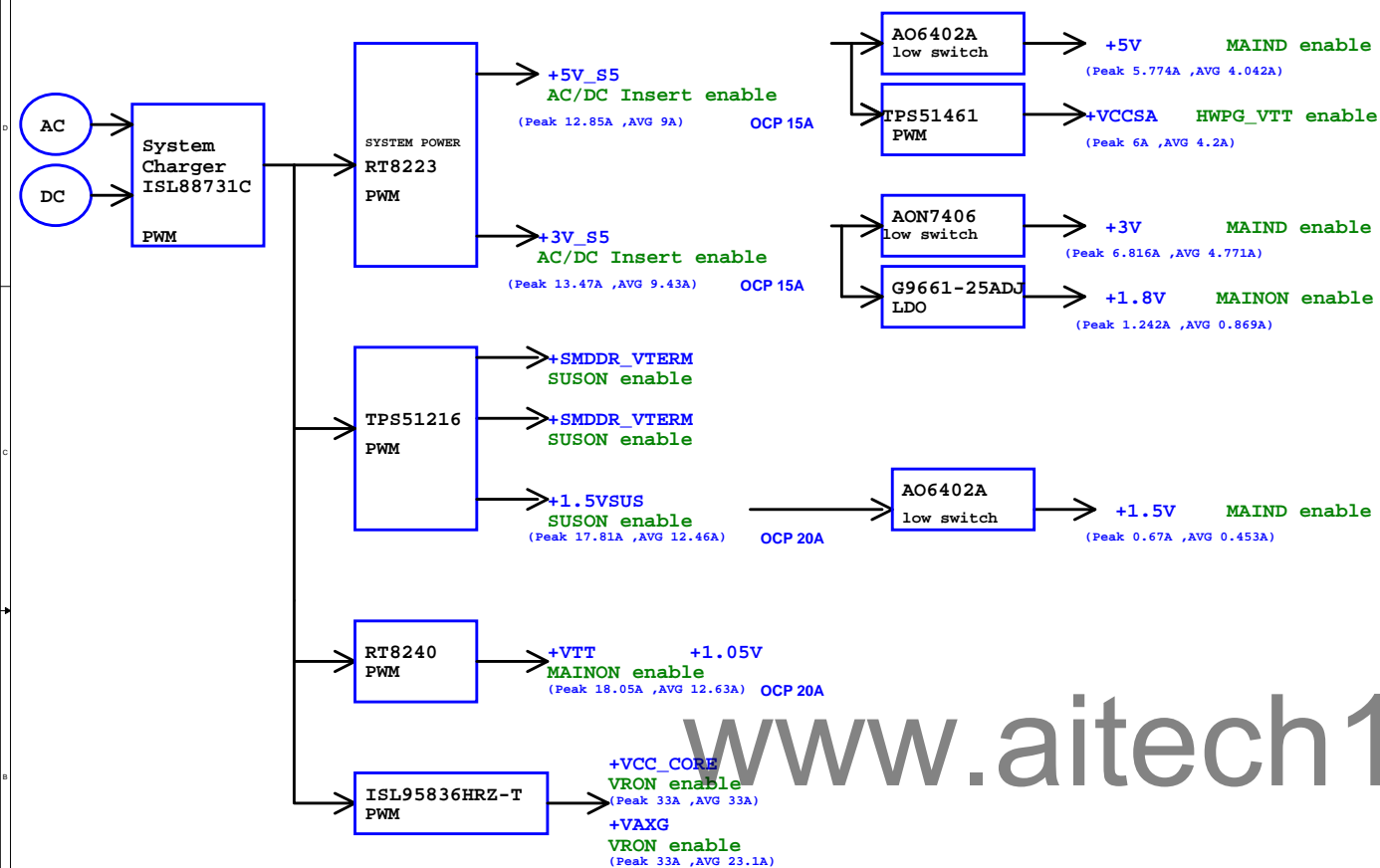


MTT Chief River Block Diagram

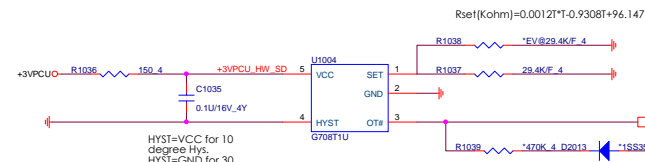
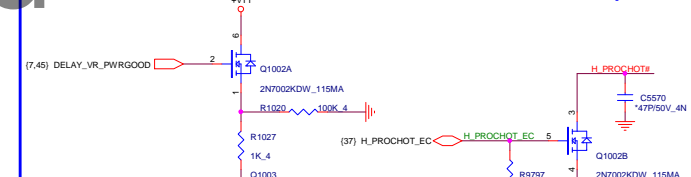
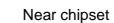
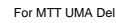
01



POWER SYSTEM		
Charger	(ISL88731C)	P40
System 5V/3V	(TPS51123A)	P41
DDR1.5V	(TPS51216)	P42
VTT	(RT8240BGQW)	P43
+VCCSA	(TI51461)	P44
+VCORE+VGFX	(ISL95836)	P45
+1.8V	(G966A)	P46
AMD_GPU	(ISL95870A)	P47

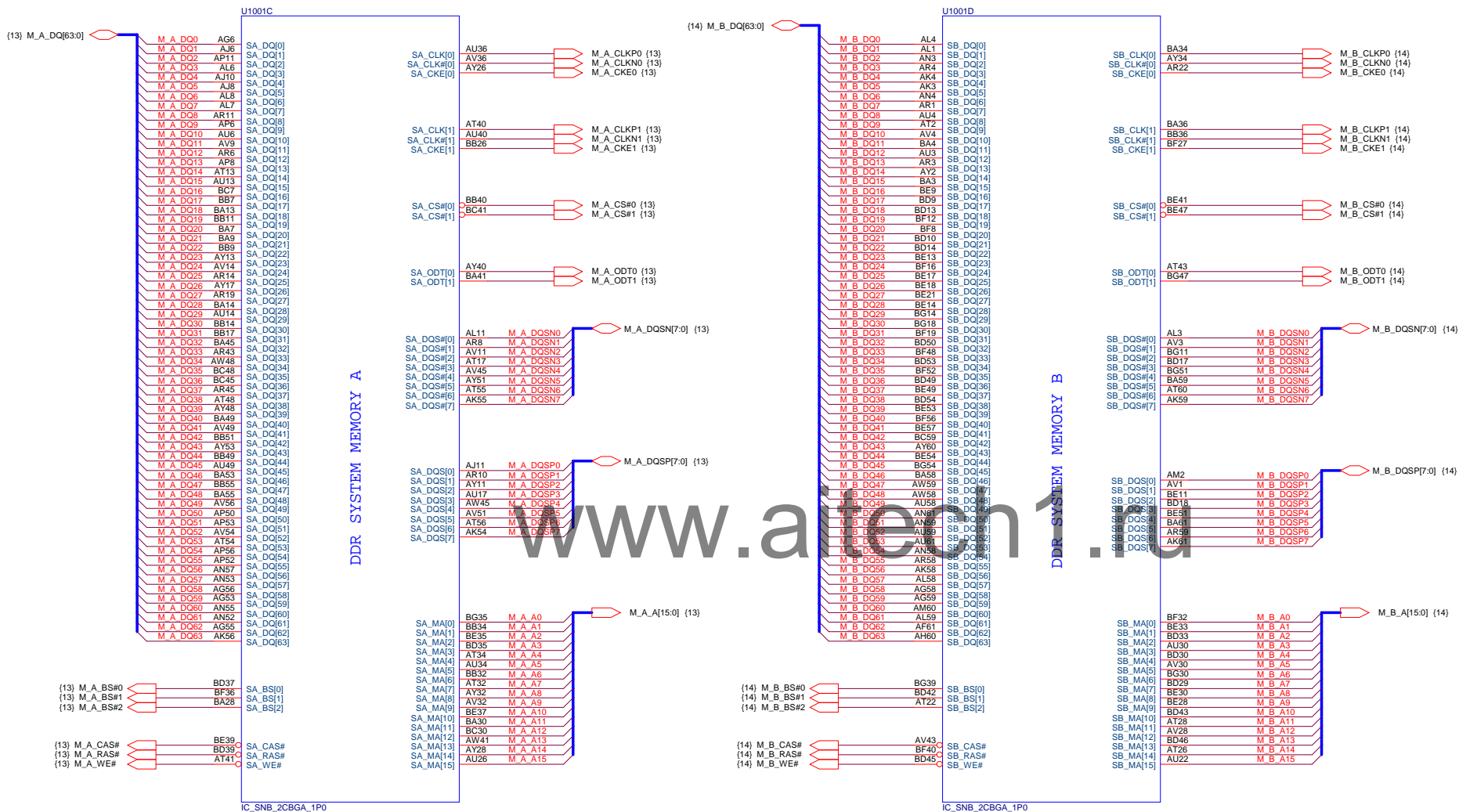


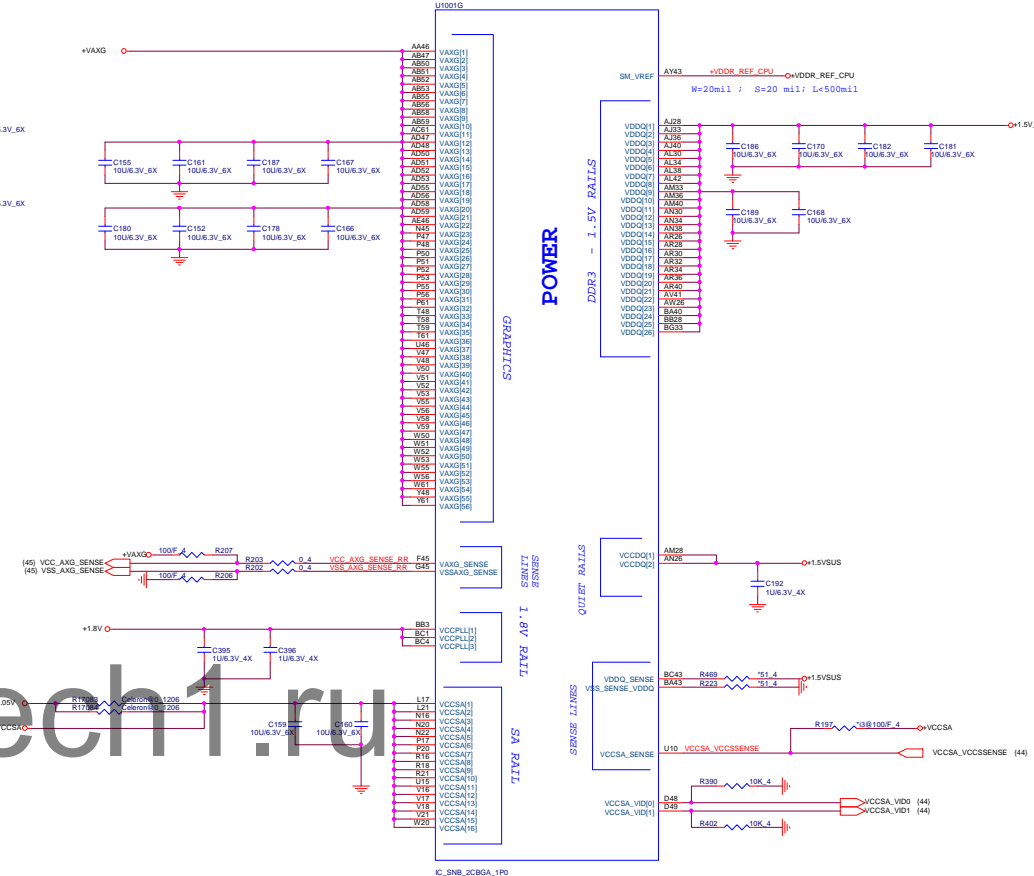
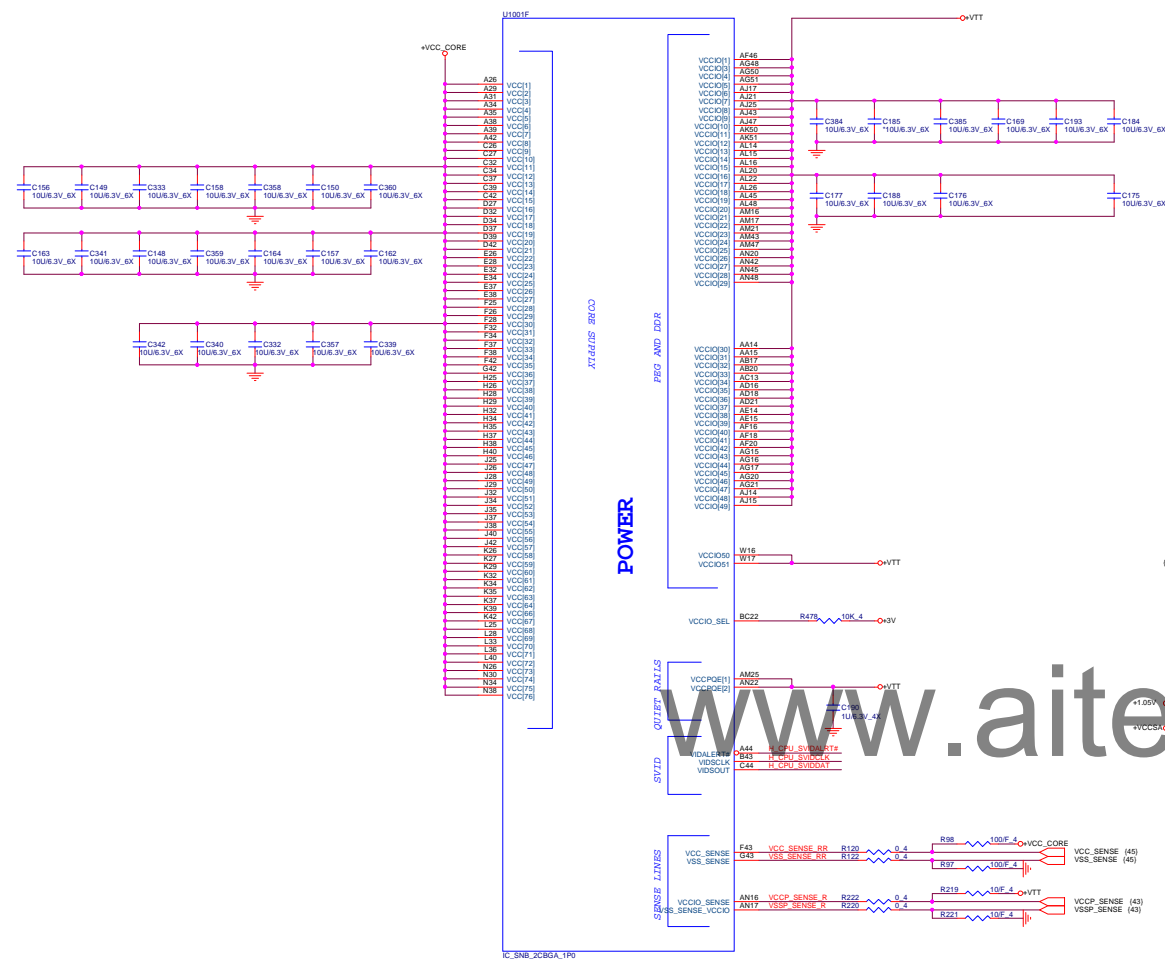
POWER PLANE	VOLTAGE	CONTROL SIGNAL	Power States ACTIVE IN
VIN	10V~+19V		S0-S5
+VCCRTC	+3.0V~+3.3V		S0-S5
+3V	+3.3V	MAIN_ON	S0
+3V_S5	+3.3V	S5_ON	S0-S5
+3V_HDP	+3.3V	MAIN_ON	S0
+3VPCU	+3.3V	AC/DC Insert enable	S0
+5V	+5V	MAIN_ON	S0
+5V_S5	+5V	S5_ON	S0-S5
+5VPCU	+5V	AC/DC Insert enable	S0-S5
WIMAX_P	+3.3V	WMAX_P for WLAN	
+1.8V	+1.8V	MAIN_ON	S0
+1.5V	+1.5V	MAIN_ON	S0
+1.5V_SUS	+1.5V	SUSON	S0-S3
+VCC_CORE		VRON	S0
+VTT	+1.05V	MAIN_ON	S0
+1.05V	+1.05V	MAIN_ON	S0
+VAXG		MPWROK	S0



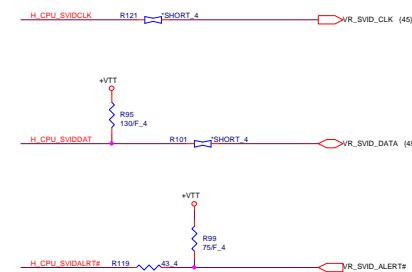
Ivy/Sandy Bridge Processor (DDR3)

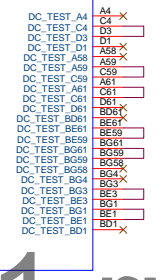
04





Layout note: need routing together and ALERT need between CLK and DATA



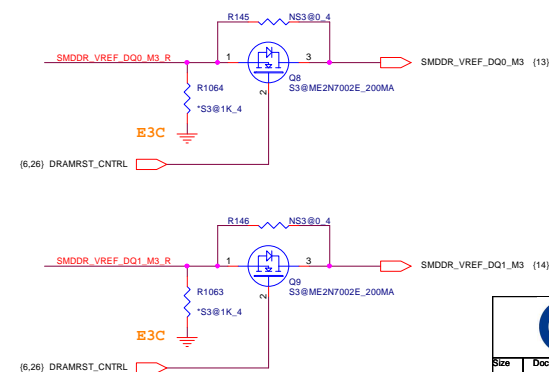


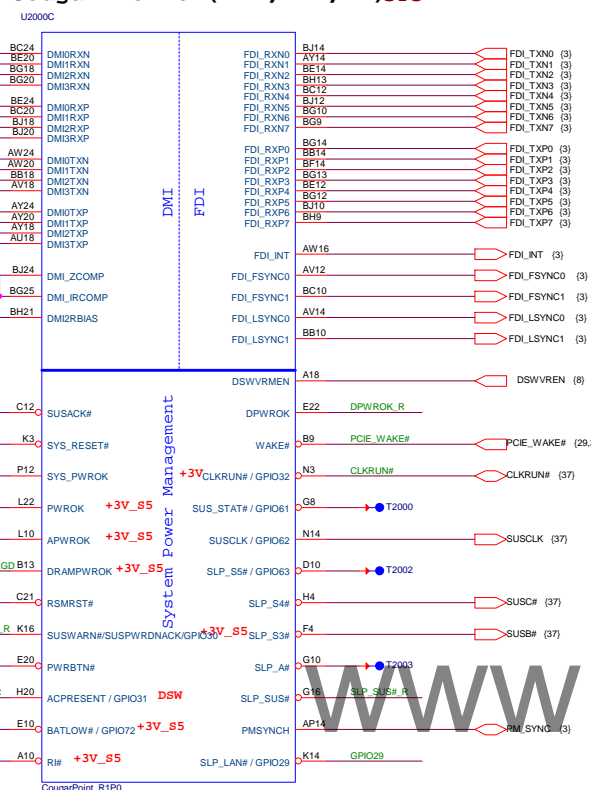
VSS152 A789
 VSS153 A19
 VSS154 BA1
 VSS155 BA11
 VSS156 BA7
 VSS157 BA2
 VSS158 BA32
 VSS159 BA44
 VSS160 BA51
 VSS161 BA61

IC SNB-20BGA-TP0

CFG[6:5] (PCIe Port Bifurcation Straps)

- 11: (Default) x16 - Device 1 functions 1 and 2 disabled
- 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
- 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled
- 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

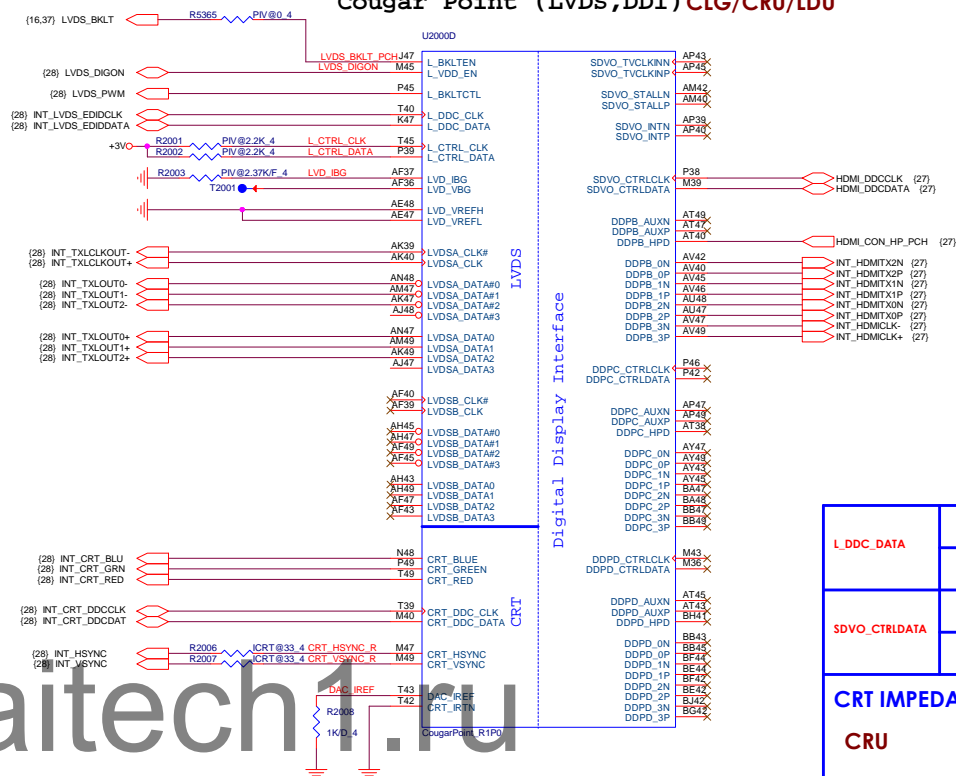


Cougar Point (DMI,FDI,PM)**CLG**

Near chipset



Cougar Point (LVDS,DDI) **CLG/CRU/LDU**



I_DDC_DATA	1 -- LVDS ENABLE
	0 -- LVDS DISABLE
SDVO_CTRLDATA	1 -- PORT B Detected
	0 -- PORT B Disable

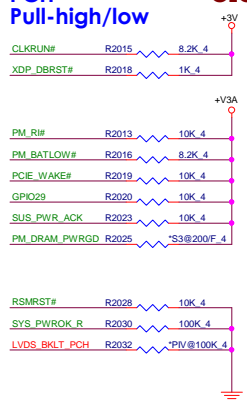
CRT IMPEDANCE MATCHING

CRL



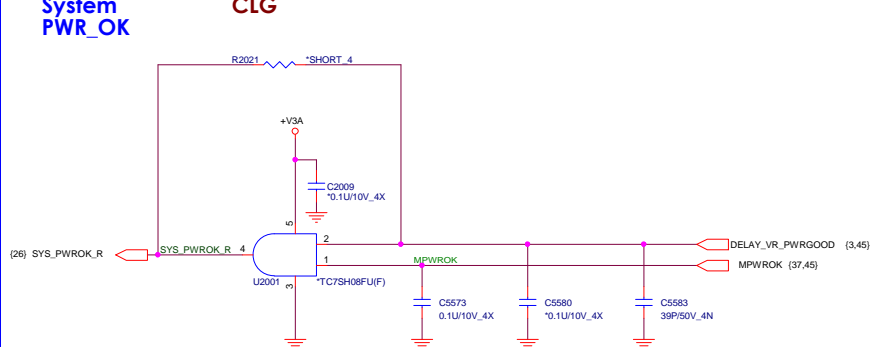
PCH
Pull-high/low

CLG/PIV/S3P

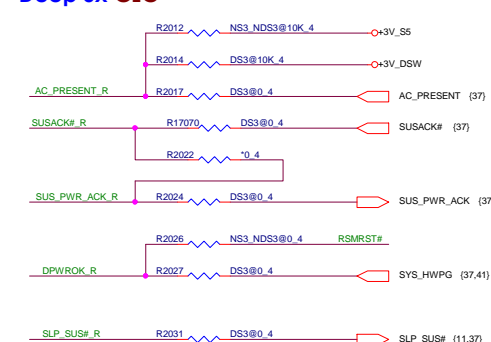


System
PWR OK

CLG



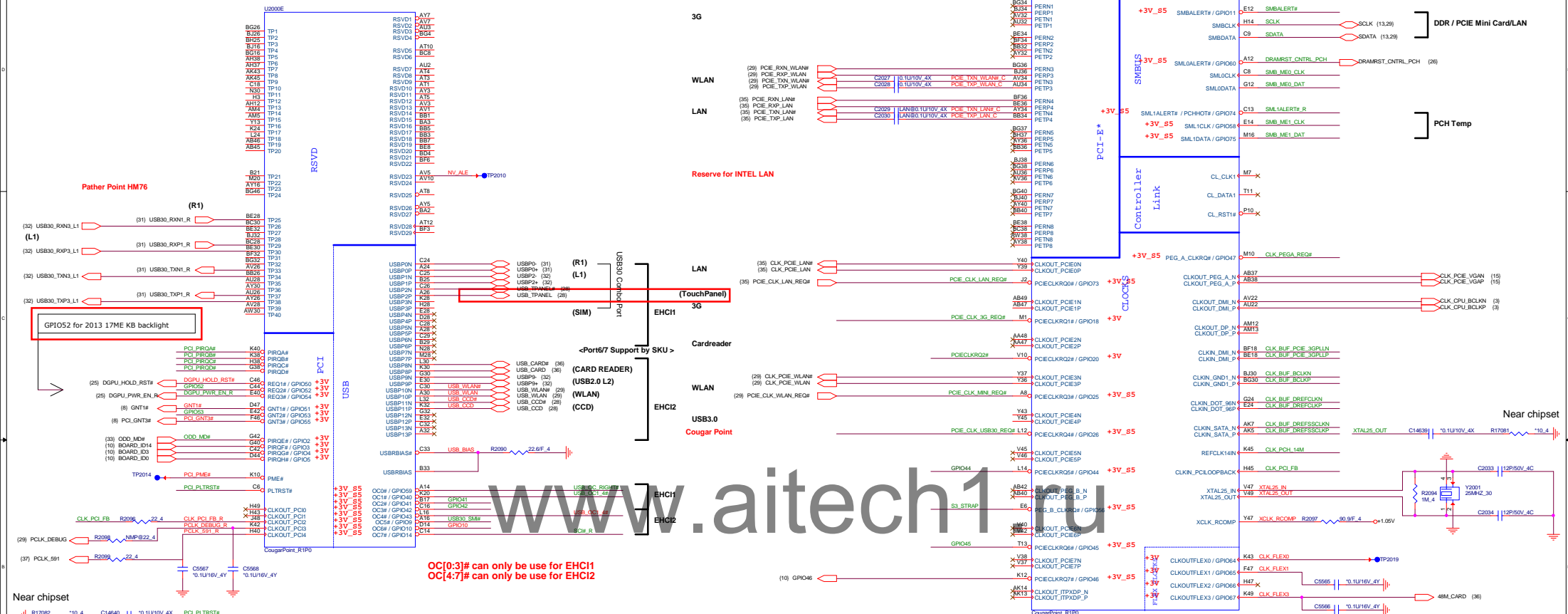
Deep Sx CLG



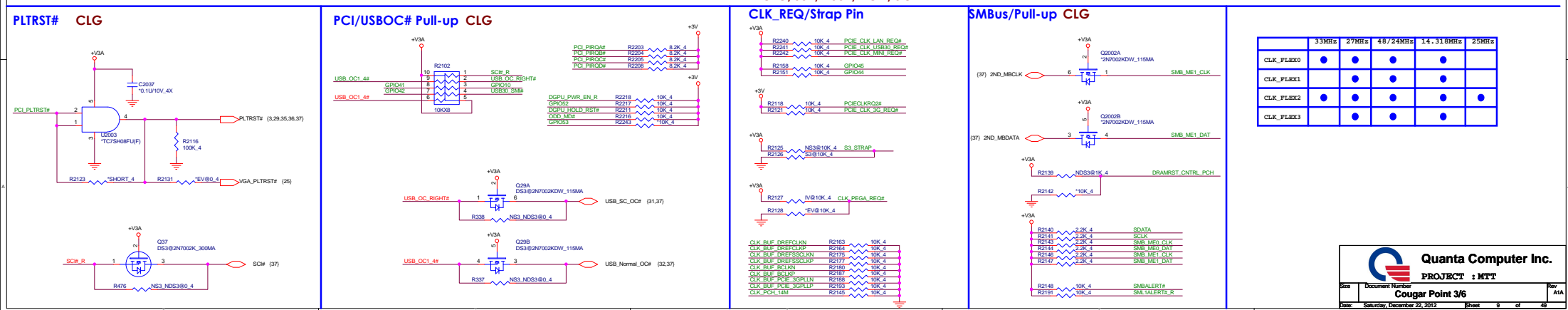
Quanta Computer Inc.
PROJECT : MTT

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	Cougar Point 1/6	A
Date	Saturday, December 22, 2012	Sheet 7 of 49

L2000E			
BG26	TP1	RSVD1	A17
B126	TP2	RSVD2	A17
B125	TP3	RSVD3	A13
B116	TP4	RSVD4	A13
B610	TP6	RSVD5	A13
AH38	TP6	RSVD6	A10
AH37	TP6	RSVD7	A10
AH34	TP7		
AH35	TP8		
C18	TP9	A12	A12
N30	TP10	RSVD1	A14
N33	TP11	RSVD2	A17
AH12	TP12	RSVD3	A11
AH4	TP13	RSVD4	A15
AH11	TP14	RSVD1	A13
AH4	TP15	RSVD2	A11
AH5	TP16	RSVD3	B11
K24	TP16	RSVD4	B13
K24	TP16	RSVD5	B15
K24	TP16	RSVD6	B17
AH50	TP19	RSVD7	B18
AH45	TP20	RSVD8	B18
		RSVD9	B18

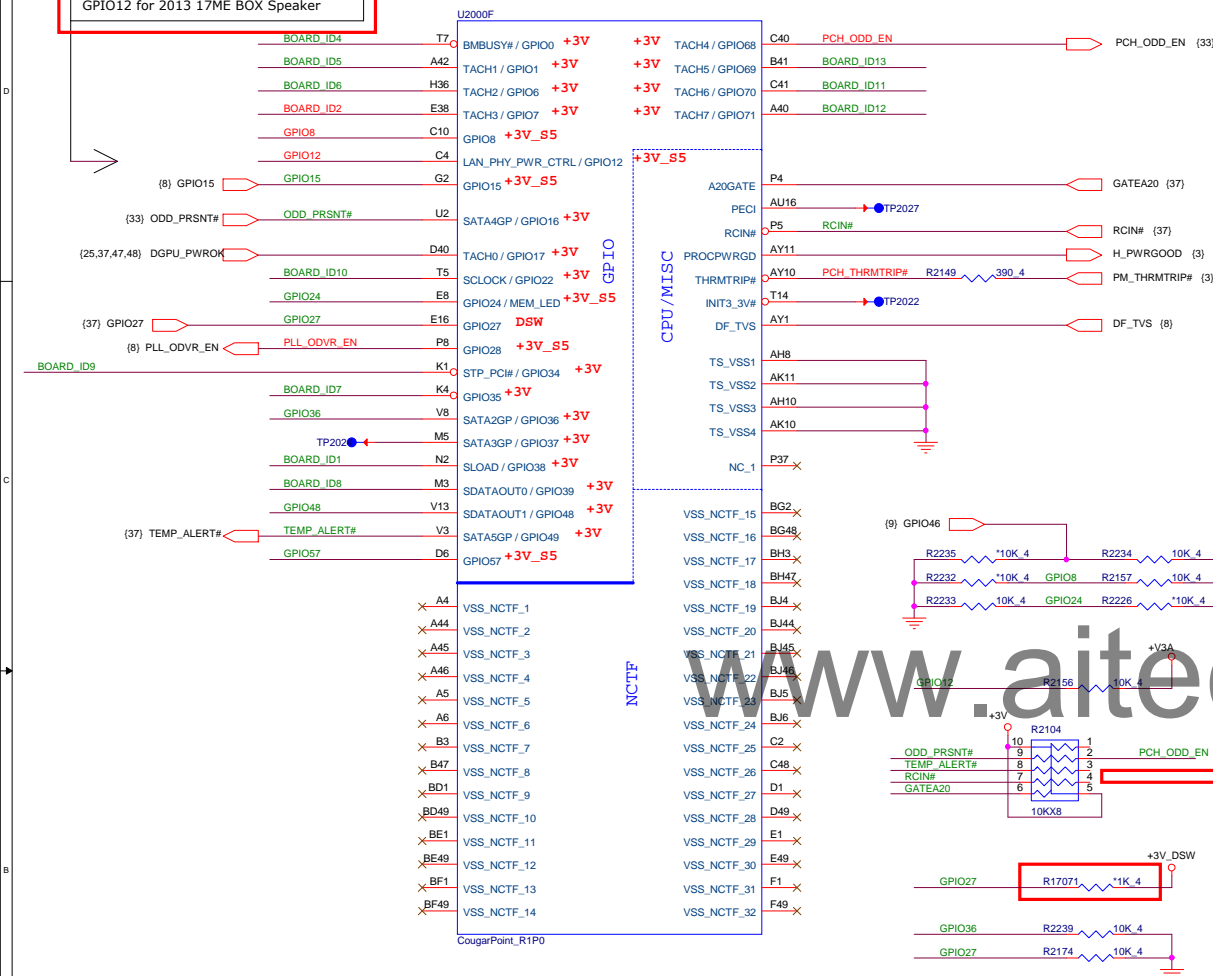


CLG/S3P/NS3P/VGA/UGA



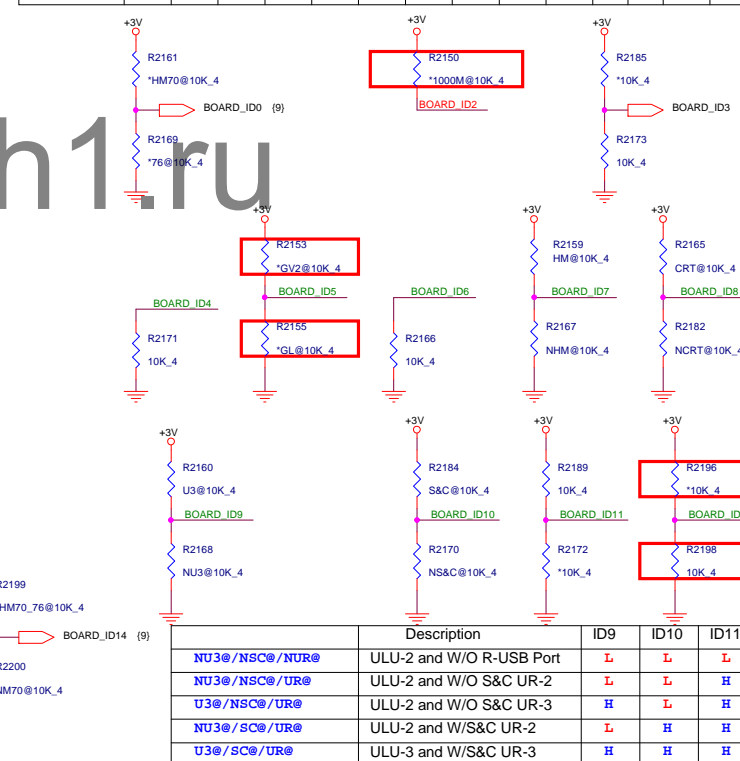
Cougar Point (GPIO,VSS_NCTF,RSVD) CLG

GPIO12 for 2013 17ME BOX Speaker



BOARD ID SETTING CLG/PX/OEV/UGA/CLG-Strap

Board ID	ID0	ID1	ID2	ID3	ID4	ID5	ID6	ID7	ID8	ID12	ID13	ID14	ID16	ID17
HM70	H	L												
UMA SKU		H	L											
VGA SKU														
VRAM-1000MHz														
VRAM-900MHz														
CF SV														
CF ULT														
17"														
14"														
GV2														
GL														
W/ G-sensor														
W/O G-sensor														
W/ HDMI														
W/O HDMI														
w CRT														
wo CRT														
Only VGA														
PX mode														
Win7(Reserve)														
Win8(Reserve)														
HM70_76														
NM70														
Celeron CPU														
i3 CPU(Reserve)														
i5(Reserve)														
i7(Reserve)														

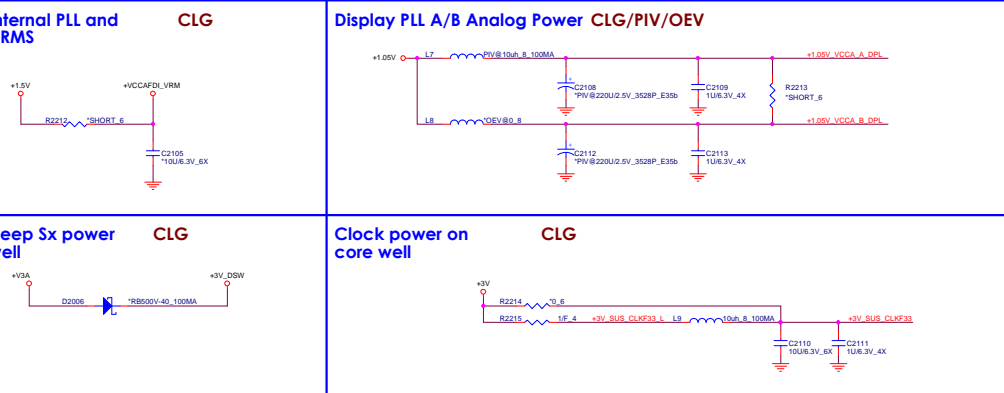
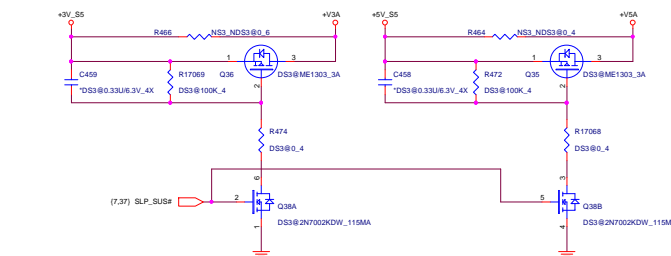
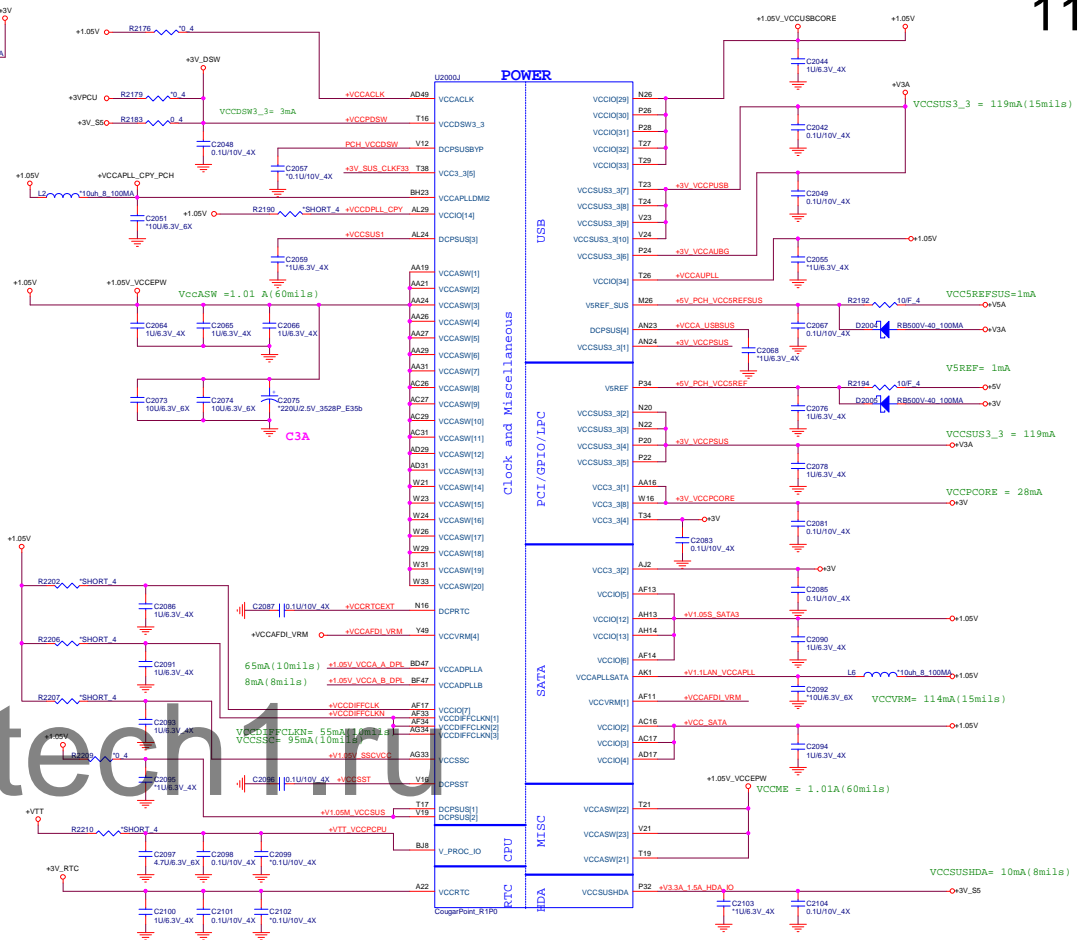


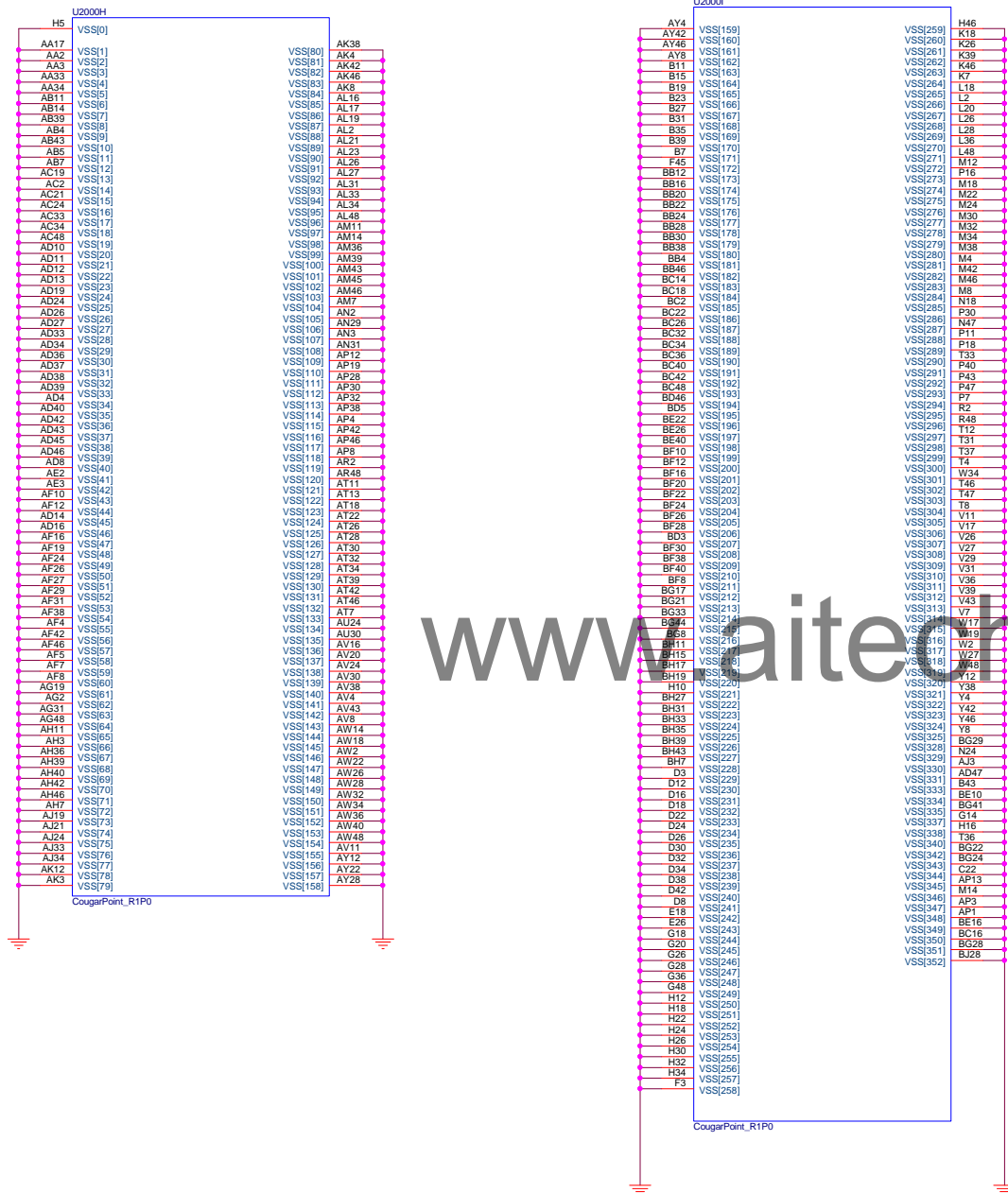
GPIO48	default
EDP	H
LVDS	L

ID_Detect	default
Metal / IMR	H
TEXTURE	L

Description	ID9	ID10	ID11
NU3@/NSC@/NUR@	L	L	L
NU3@/NSC@/UR@	L	L	H
U3@/NSC@/UR@	L	L	H
NU3@/SC@/UR@	L	H	H
U3@/SC@/UR@	H	H	H

U3@ S&C@ UR@
NU3@ NS&C@ NUR@

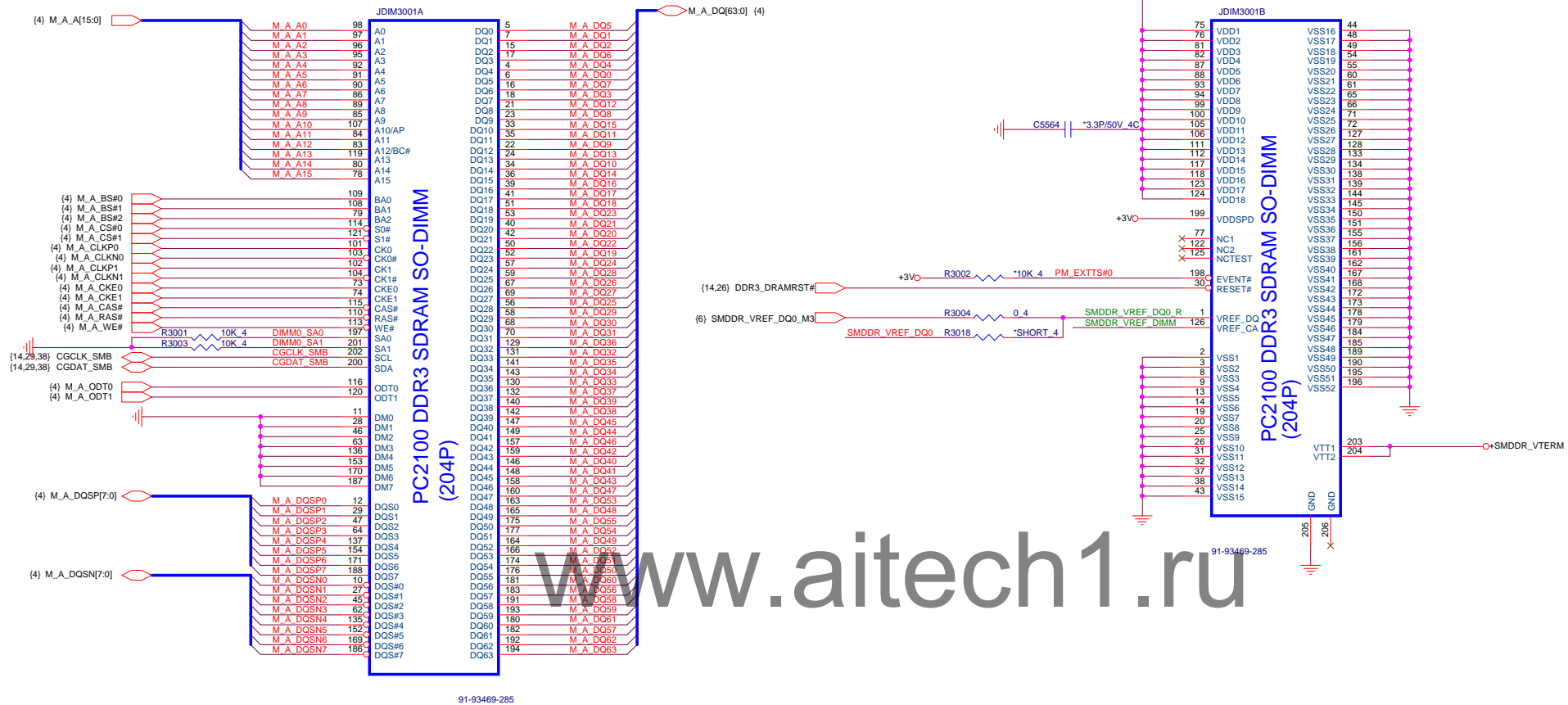




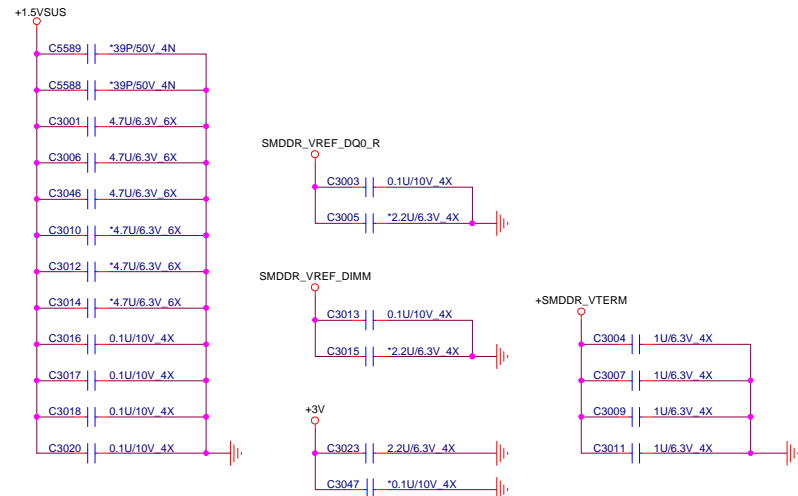
Quanta Computer Inc.

PROJECT : MTT

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	Cougar Point 6/6	A1A
Date	Saturday, December 22, 2012	Sheet 12 of 46

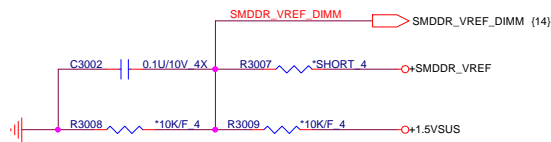


DDR Power Decoupling DDR



DDR3 VREF CA

DDR

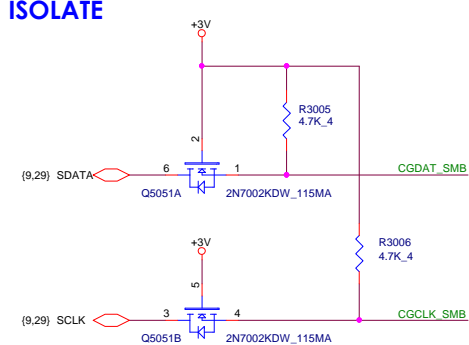


DDR3 VREF DQ (M1) DDR

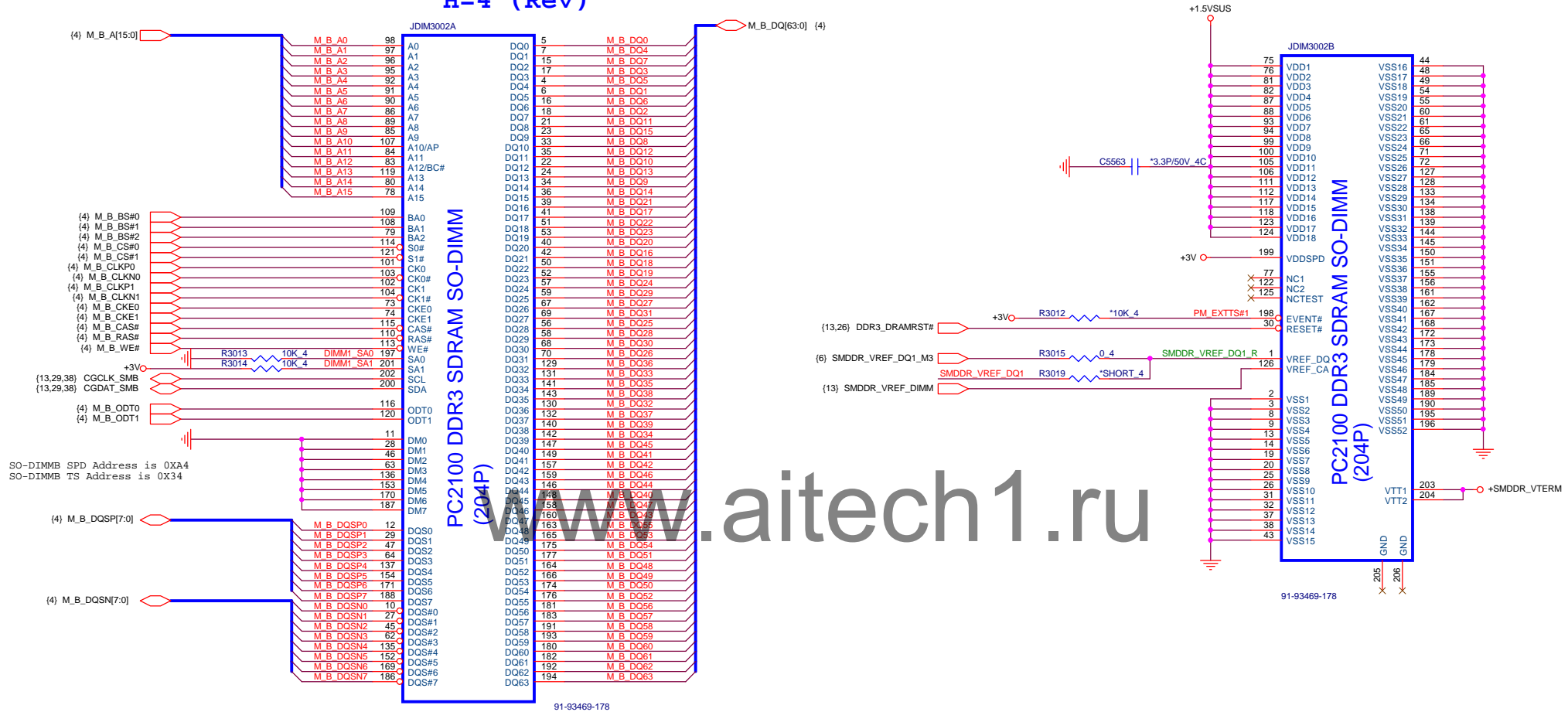


SMBUS ISOLATE

DDR



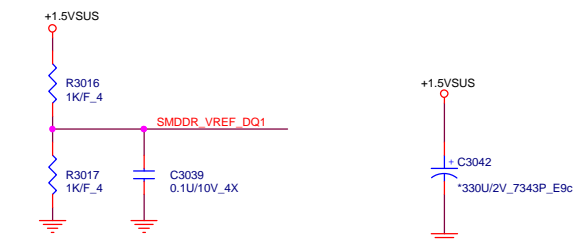
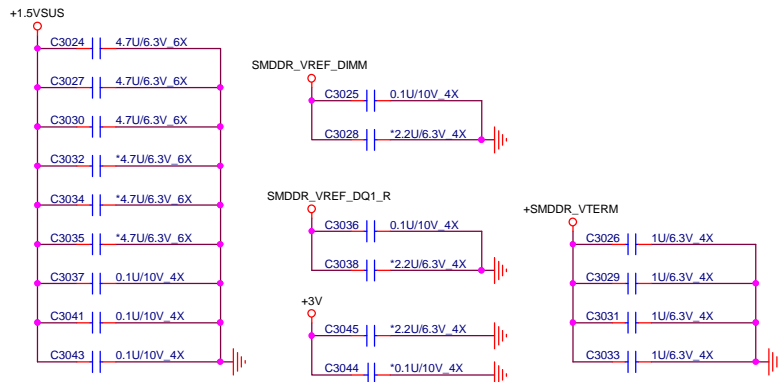
H=4 (Rev)



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DDR Power Decoupling DDR

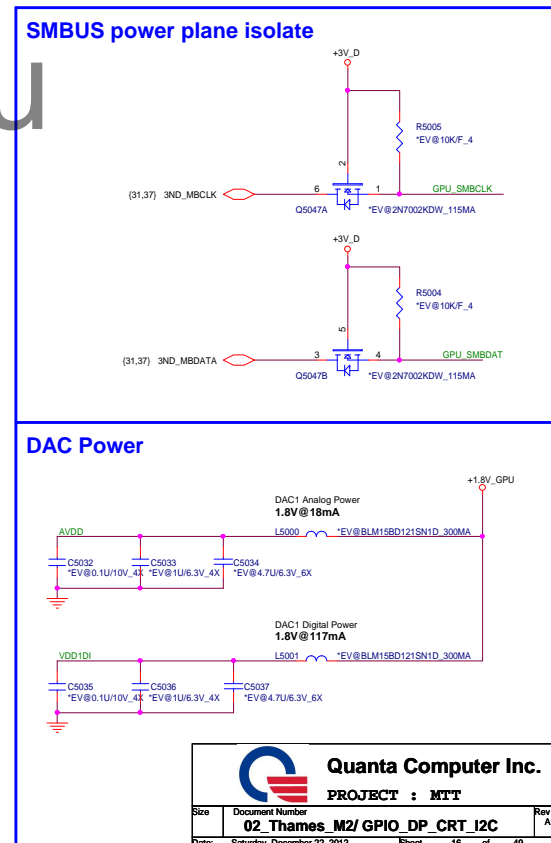
DDR3 VREF DQ (M1) DDR

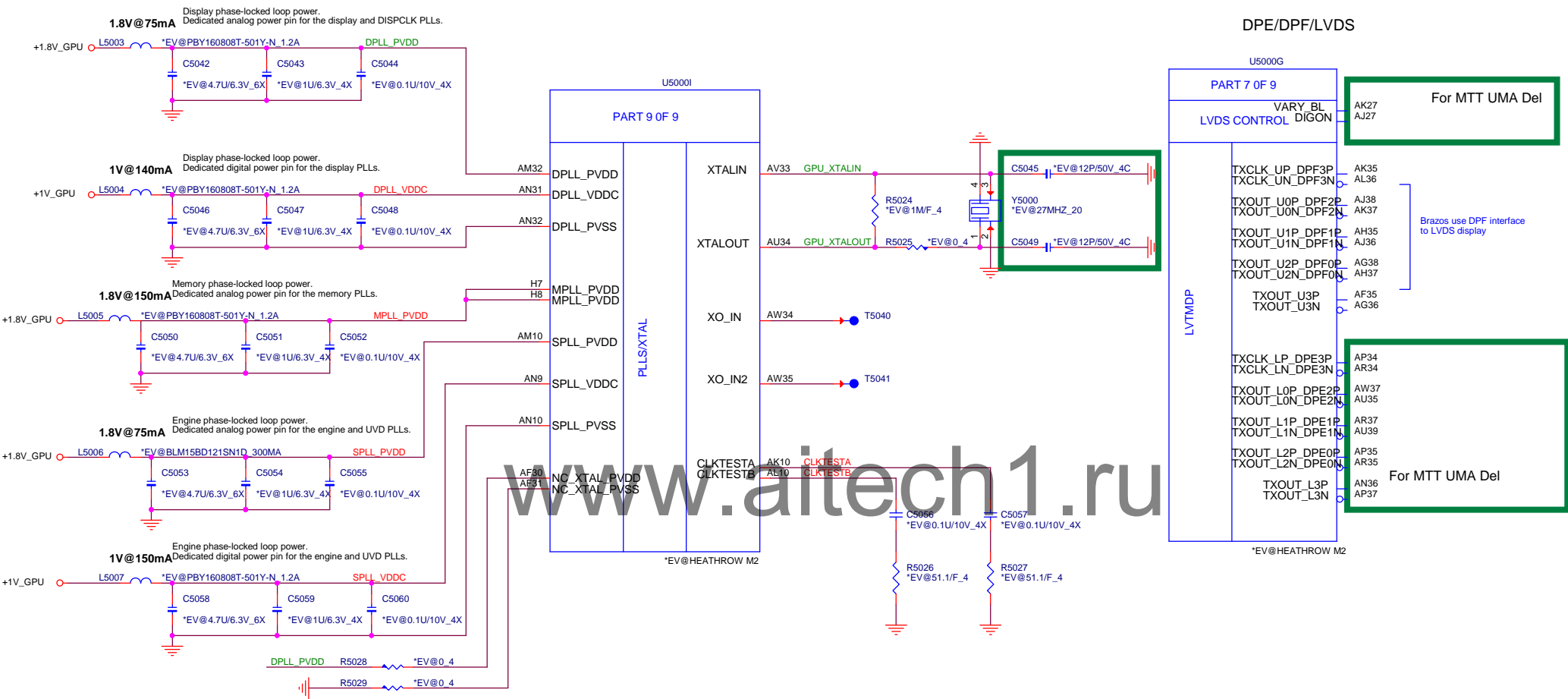


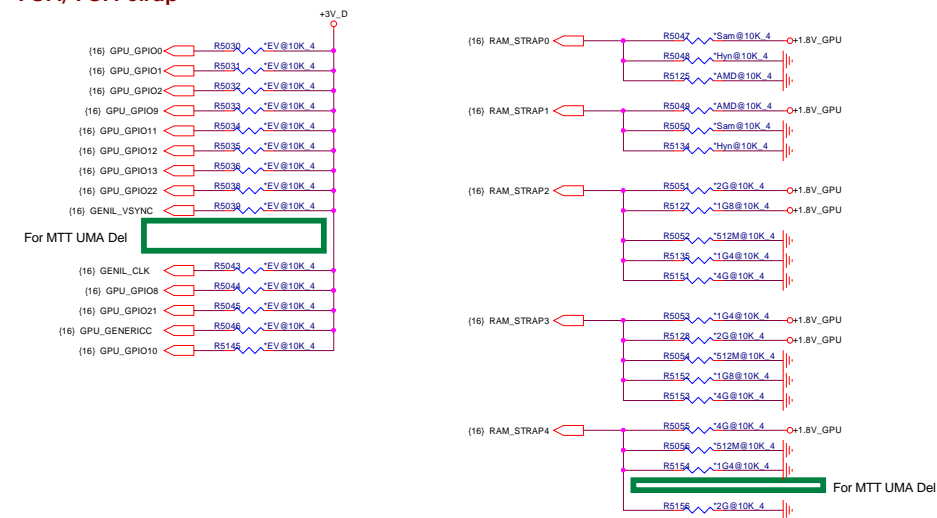


1 => +1V_GPU
2 => +3V_D
3 => +VGPU_CORE,+1.5V_GPU
4 => +1.8V_GPU

Intel platform: Lane0 ~ Lane15
Brazos platform: Lane12 ~ Lane15
Comal and Sabine platform: Lane8 ~Lane15







DDR3 Memory TYPE				Size			Vendor	
Vendor	Vendor P/N	STN B/S P/N	Size	RAM_STRAP4 DVDPDATA_4	RAM_STRAP3 DVDPDATA_3	RAM_STRAP2 DVDPDATA_2	RAM_STRAP1 DVDPDATA_1	RAM_STRAP0 DVDPDATA_0
Hynix	H5TQ1G63DFR-11C (64M*16)	AKD5LZW7W02 * 4	512MB	0	0	0	0	0
		AKD5LZW7W02 * 8	1GB	0	0	1	0	0
	H5TQ2G63BFR-11C (128M*16)	AKD5MGW7W00 * 4	1GB	0	1	0	0	0
		AKD5MGW7W00 * 8	2GB	0	1	1	0	0
	H5TQ4G***** (256M*16)	AK***** * 8	4GB	1	0	0	0	0
Samsung	K4W1G1646G-BC11 (64M*16)	AKD5EGGT500 * 4	512MB	0	0	0	0	1
		AKD5EGGT500 * 8	1GB	0	0	1	0	1
	K4W2G1646C-HC11 (128M*16)	AKD5MGW7500 * 4	1GB	0	1	0	0	1
		AKD5MGW7500 * 8	2GB	0	1	1	0	1
	K4W4G***** (256M*16)	AK***** * 8	4GB	1	0	0	0	1
AMD	23EY2387MC11 (64M*16)	AKD5EZW7700 * 4	512MB	0	0	0	1	0
		AKD5EZW7700 * 8	1GB	0	0	1	1	0
	23EY4187MC11 (128M*16)	AKD5DZW7700 * 4	1GB	0	1	0	1	0
		AKD5DZW7700 * 8	2GB	0	1	1	1	0
	23EY***** (256M*16)	AK***** * 8	4GB	1	0	0	1	0

512@ & Hyn@

1GB@ & Hyn@

1GB@ & Hyn@

2GB@ & Hyn@

4GB@ & Hyn@

512@ & Sam@

1GB@ & Sam@

1GB@ & Sam@

2GB@ & Sam@

4GB@ & Sam@

512@ & AMD@

1GB@ & AMD@

1GB@ & AMD@

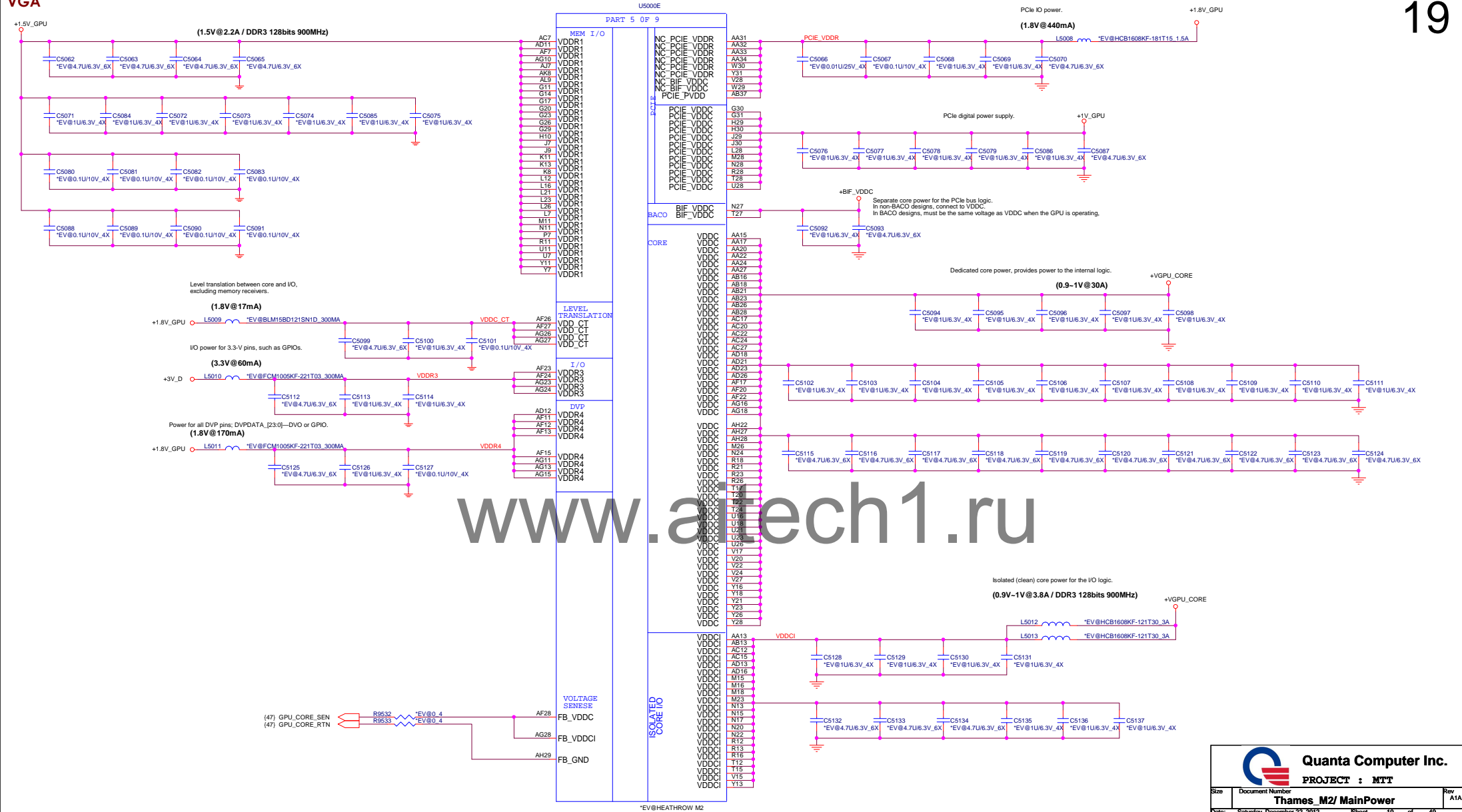
2GB@ & AMD@

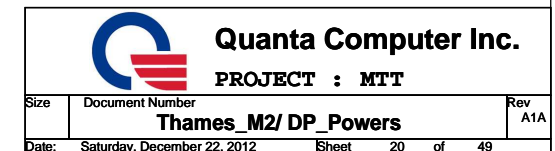
4GB@ & AMD@

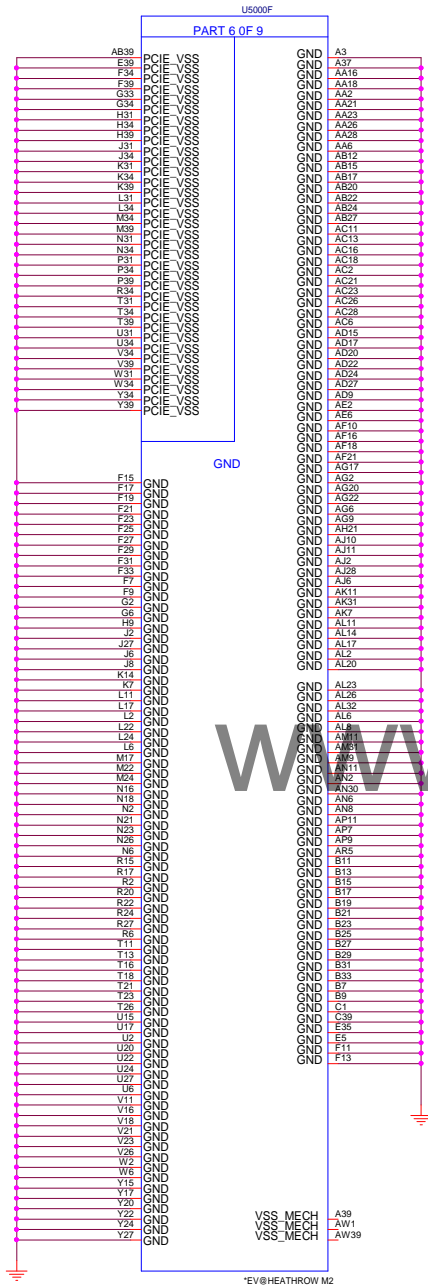
CONFIGURATION STRAPS – SEE EACH DATABASE FOR STRAP DETAILS ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET				MB Default Setting(I/C internal PD)	
STRAPS	MLPS	GPIO PIN	DESCRIPTION OF DEFAULT SETTINGS		
MLPS_DISABLE	NA	GPIO_28_FDO	Enable MLPS. NA for Thames/Whistler/Seymour 0: Enable MLPS, disable GPIO PINSTRAP 1: Disable MLPS, enable GPIO PINSTRAP	1	
TX_PWRS_ENB	PS_1[4]	GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing 1: Full Tx output swing	1	
TX_DEEMPH_EN	PS_1[5]	GPIO1	PCIE Transmitter De-emphasis Enable 0: Tx de-emphasis disabled 1: Tx de-emphasis enabled	1	
BIF_GEN3_EN_A	PS_1[1]	GPIO2	PCIE Gen3 Enable (NOTE: RESERVED for Thames/Whistler/Seymour) 0: GEN3 not supported at power-on 1: GEN3 supported at power-on	0	
BIF_VGA_DIS	PS_2[4]	GPIO9	VGA Control 0: VGA controller capacity enabled 1: VGA controller capacity disabled (for multi-GPU)	0	
ROMIDCFG[2:0]	PS_0[3..1]	GPIOQ[13:11]	Serial ROM type or Memory Aperture Size Select If GPIO22 = 0, defines memory aperture size If GPIO22 = 1, defines ROM type 100 - 512Kbit M25P05A (ST) 101 - 1Mbit M25P10A (ST) 101 - 2Mbit M25P20 (ST) 101 - 4Mbit M25P40 (ST) 101 - 8Mbit M25P80 (ST) 100 - 512Kbit Pm25LV512 (Chingis) 101 - 1Mbit Pm25LV010 (Chingis)	XXX	
BIOS_ROM_EN	PS_2[3]	GPIO22	Enable external BIOS ROM device 0: Disabled 1: Enabled	0	
AUD[1] AUD[0]	NA NA	HSYNC VSYNC	00 - No audio function 01 - Audio for DP only 10 - Audio for DP and HDMI if dongle is detected 11 - Audio for both DP and HDMI HDMI must only be enabled on systems that are legally entitled. It is the responsibility of the system designer to ensure that the system is entitled to support this feature.	XX	
CEC_DIS	PS_0[4]	GENLK_VSYNC	Enable CEC function. Reserved for Thames/Whistler/Seymour 0: Disabled 1: Enabled	0	
RESERVED RESERVED RESERVED RESERVED	PS_1[3] PS_1[2] NA NA	GENLK_CLK GPIO8 GPIO21 GENERICC	NOTE: ALLOW FOR PULLUP PADS FOR THE RESERVED STRAPS BUT DO NOT INSTALL RESISTOR IF THESE GPIOs ARE USED, THEY MUST KEEP LOW AND NOT CONFLICT DURING RESET	0 0 0 0	
AUD_PORT_CONN_PINSTRAP0 AUD_PORT_CONN_PINSTRAP1 AUD_PORT_CONN_PINSTRAP2	PS_3[5] PS_3[4] PS_0[5]	NA NA NA	STRAPS TO INDICATE THE NUMBER OF AUDIO CAPABLE DISPLAY OUTPUTS 111 = 0 usable endpoints 110 = 1 usable endpoints 101 = 2 usable endpoints 100 = 3 usable endpoints 011 = 4 usable endpoints 010 = 5 usable endpoints 001 = 6 usable endpoints 000 = all endpoints are usable	XXX	

System Memory Aperture size

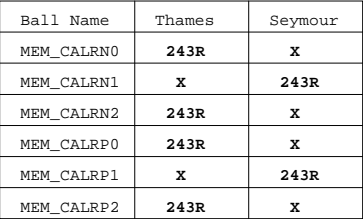
GPIO22 BIOSROM		GPIO13 ROMIDCFG2	GPIO12 ROMIDCFG1	GPIO11 ROMIDCFG0
0	128M	0	0	0
0	256M	0	0	1
0	64M	0	1	0
0	32M	0	1	1





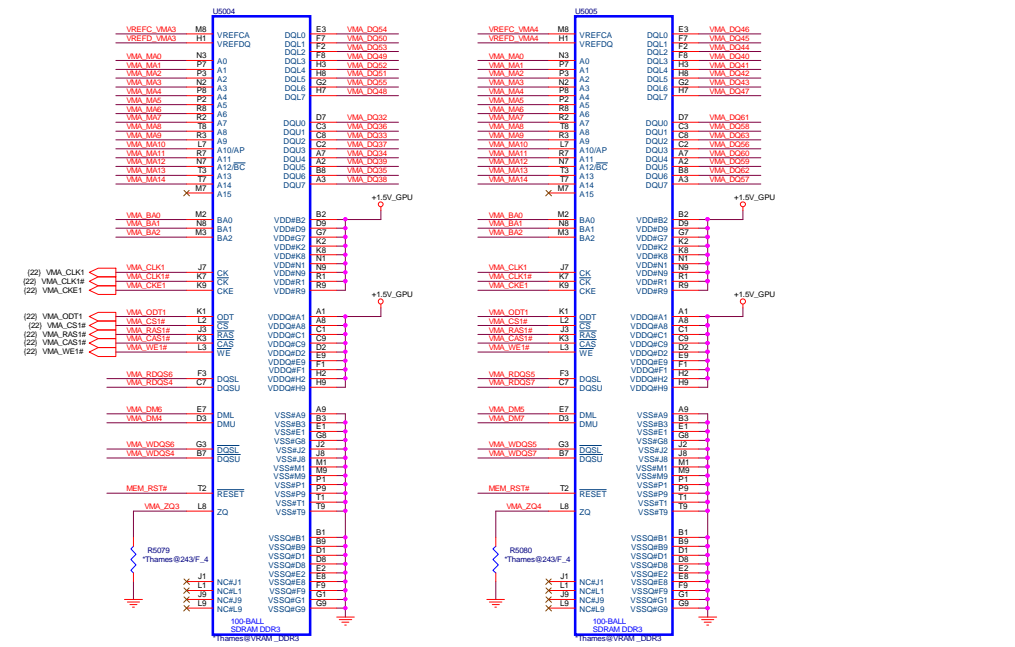


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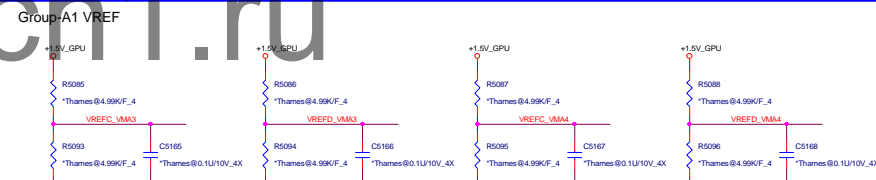


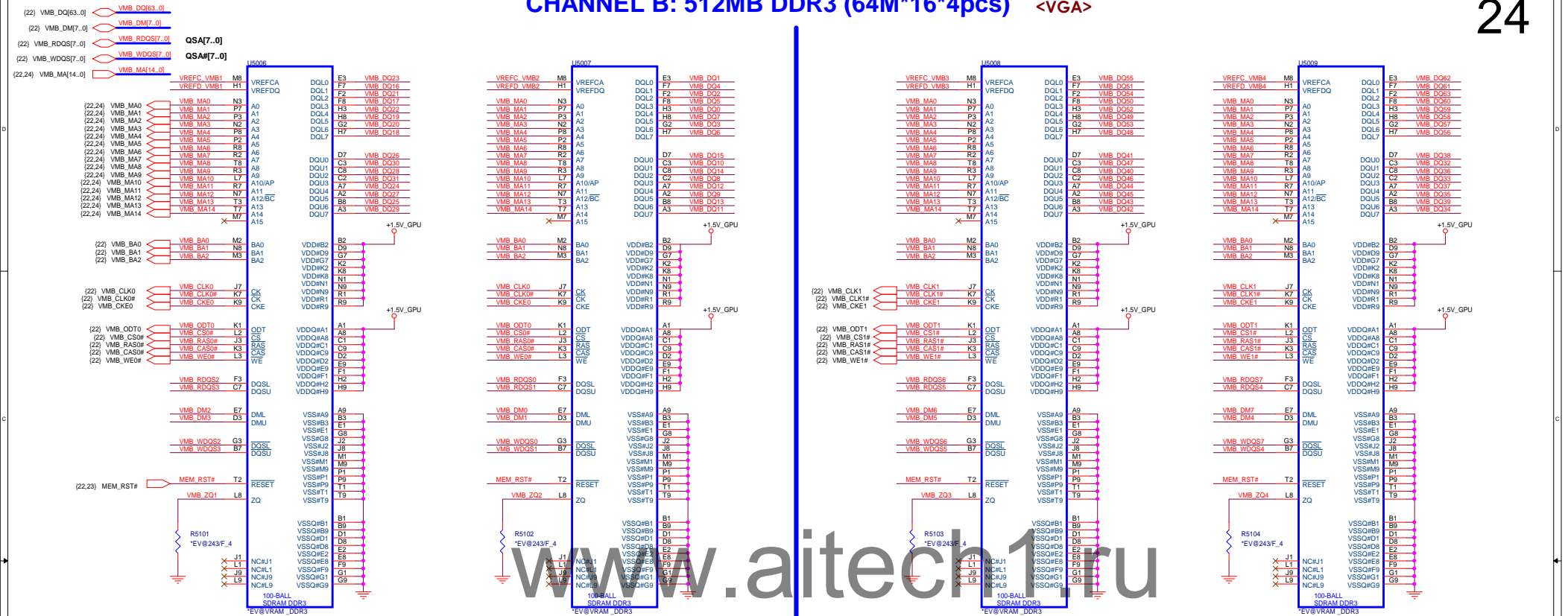
Place all these components very close to GPU (within 25mm)
and keep all components close to each other
** This basic topology should be used for DRAM_RAT for DDR3/GDDR5

These Capacitors and Resistor values are an example only
The series R and || cap values will depend on the DRAM loads
and will have to be calculated for different Memory, DRAM loads and board
to pass Reset Signal Spec



TOP Right



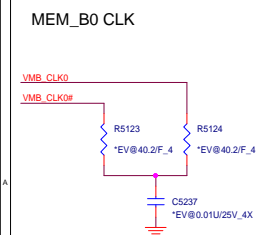
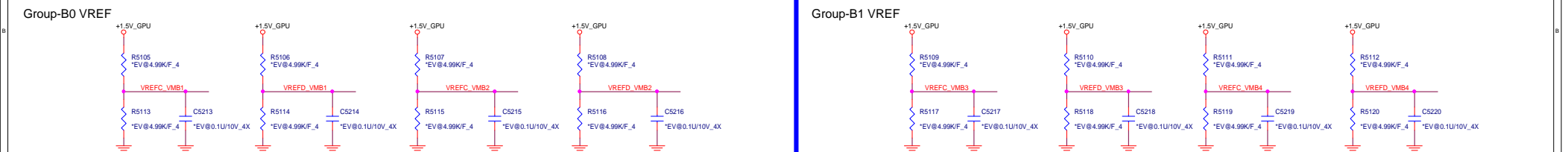


BOT Down

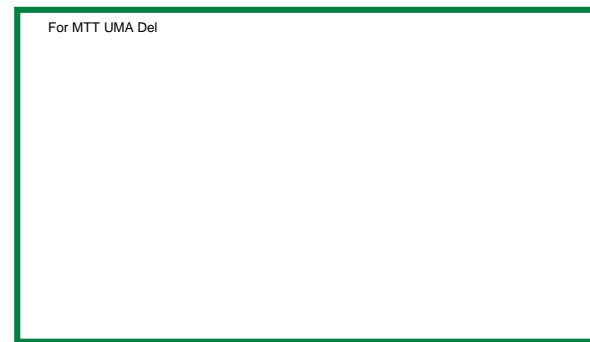
TOP Down

TOP Up

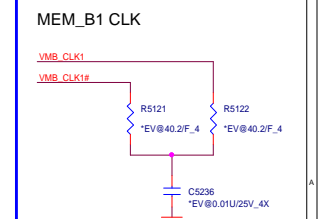
BOT Up



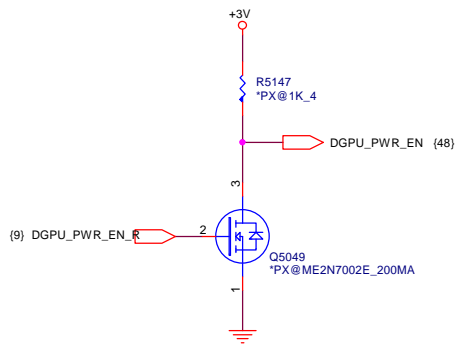
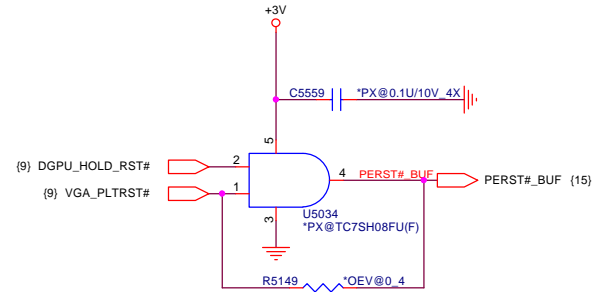
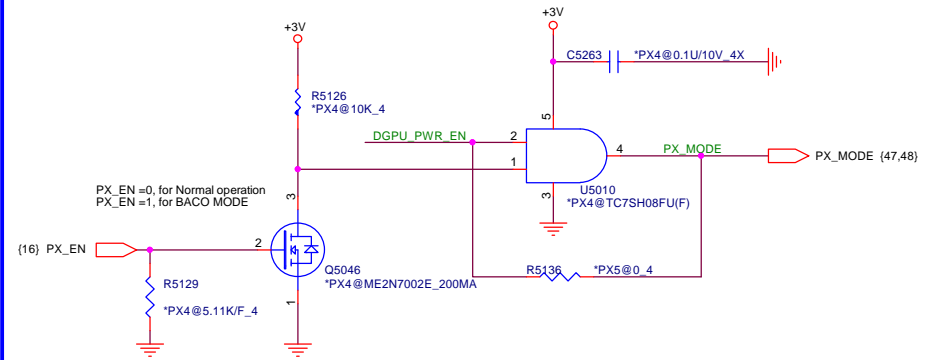
For MTT UMA Del



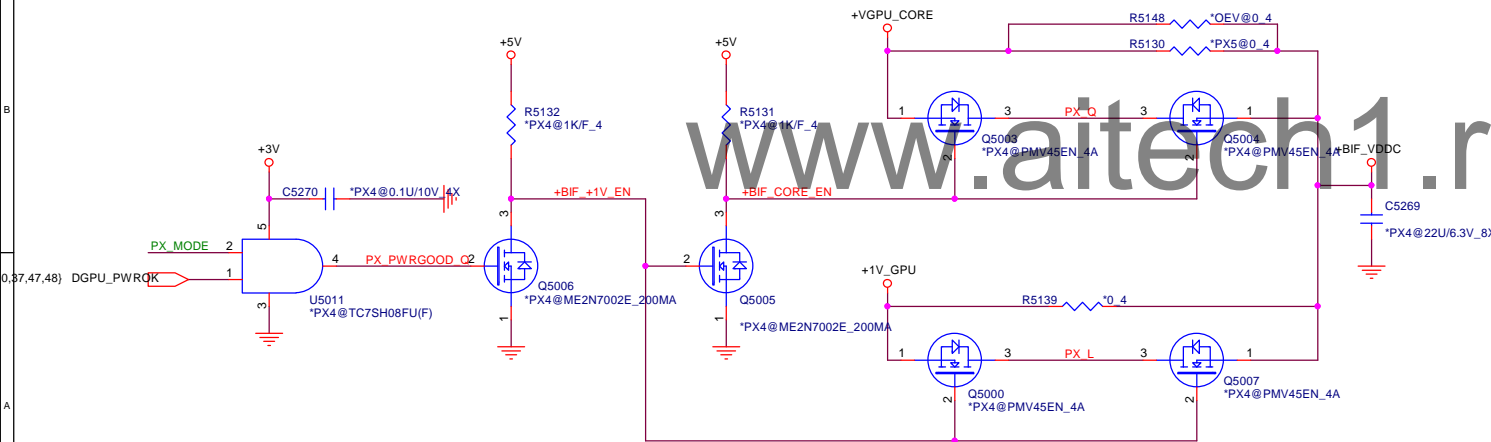
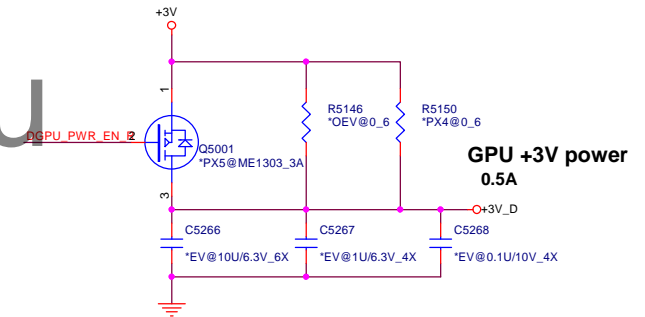
For MTT UMA Del



MEM_B1 CLK

**VGA Power Enable Reverse
(Intel --> Low Active)****PX****Platform Reset PX/OEV****PX Mode control signal PX4/PX5****Core power for PCIe Logic****PX4/PX5/OEV**

Designs that do not support the BACO option must connect the BIF_VDDC to VDDC

**3.3V VGA/PX4/PX5/OEV**

**GPU +3V power
0.5A**

**Quanta Computer Inc.****PROJECT : MTT**

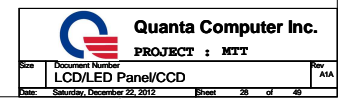
Size	Document Number	Rev
	Thames_M2/ Baco	A1A

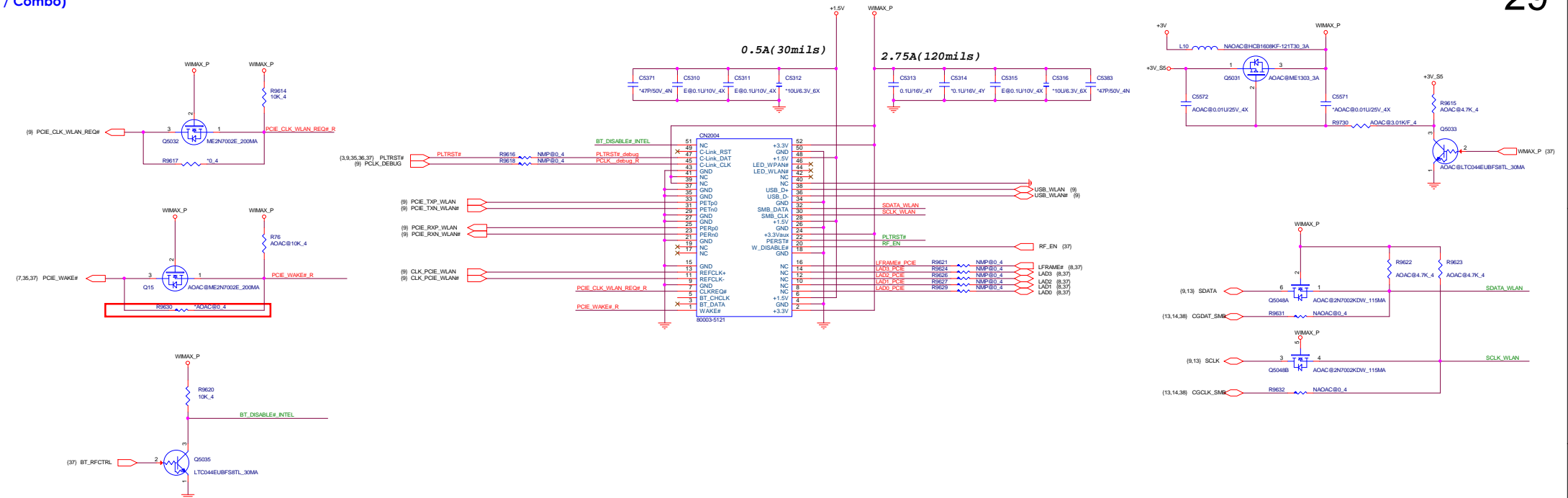
Date: Saturday, December 22, 2012 Sheet 25 of 49

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Figure 1 shows the schematic representation of the four HDMT gene constructs. Each construct is shown as a horizontal line with a blue box representing the HDMT gene. The constructs are: EXT_HDMITX2P (R4565 to *EHM@100_4), EXT_HDMITX2N (EXT_HDMITX2N), EXT_HDMITX1P (R4566 to *EHM@100_4), EXT_HDMITX1N (EXT_HDMITX1N), EXT_HDMITX0P (R4567 to *EHM@100_4), EXT_HDMITX0N (EXT_HDMITX0N), EXT_HDMCLK+ (R4571 to *EHM@100_4), and EXT_HDMCLK- (EXT_HDMCLK-).

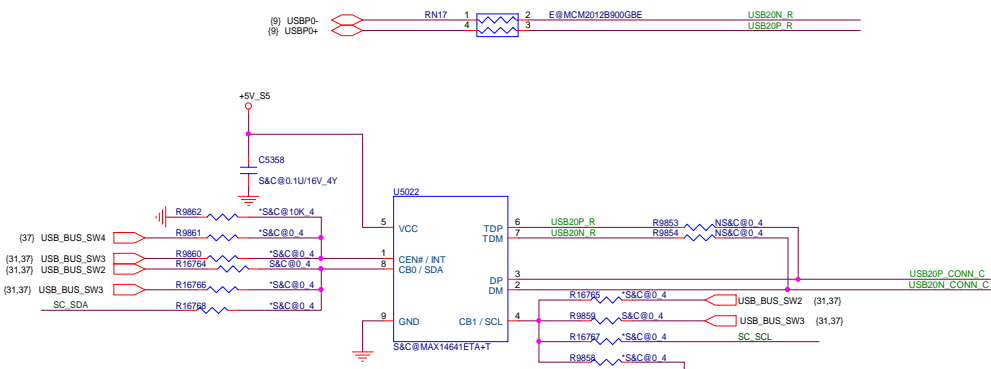




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USB CONNECT <U3B/USB> RIGHT(UR)



	R9861	R9860	R9859	R9858	R9862	R16764	R16766	R16768	R16767
14566		V		V					
14600			V			V			
14617(with CB2)	V		V						
14617(no CB2)			V		V				
14641/14642/14644			V			V			
14640								V	V

SW2	SW3	14600
CB0	CB1	Status
0	0	Auto mode
0	1	Force dedicated charger mode
1	0	Pass-Through(USB) mode
1	1	pass-through(USB) with CDP Emulation

2013 Chief River/Brazos

Charger , AM
Charger , FM
USB , PM
USB , CM

SW3	SW2	14641
CB1	CB0	Status
0	0	2A Auto mode for Apple device
1	0	Force 1A for Apple device
0	1	Pass-Through(USB) mode
1	1	pass-through(USB) with CDP Emulation

2013 Shark bay / Kabini

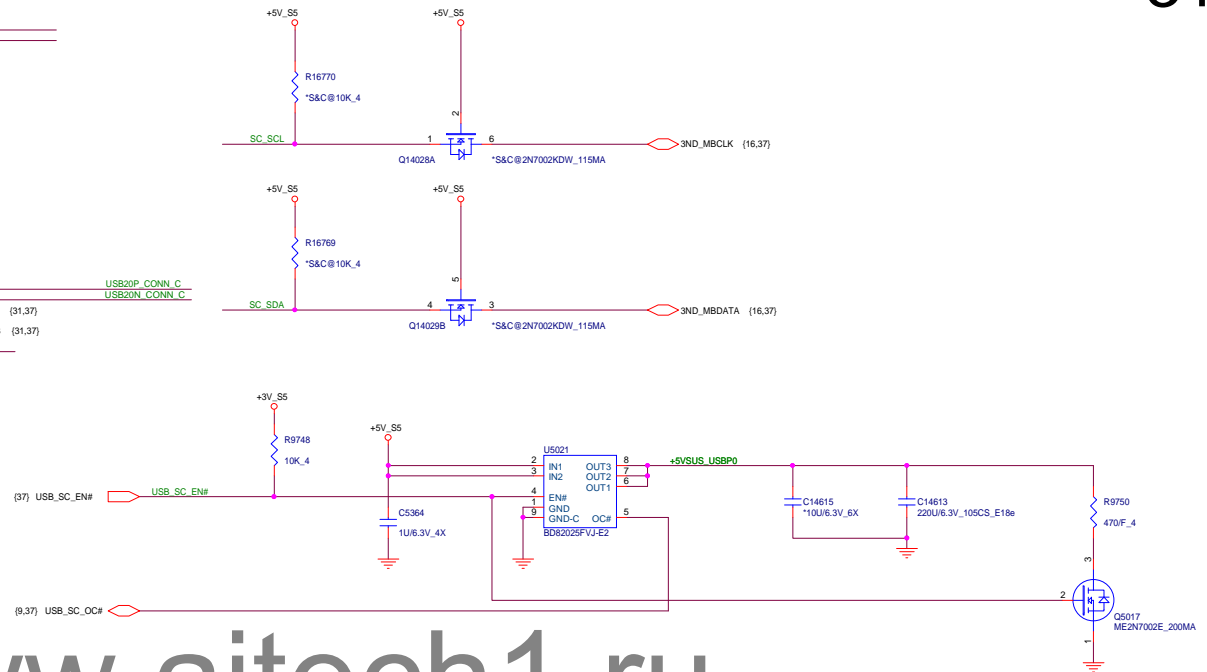
Charger , AM2
Charger , AP1
USB , PM
USB , CM

SW3	SW2	14644
CB1	CB0	Status
0	0	2A Auto mode for Apple device
1	0	Force dedicated charger mode
0	1	Pass-Through(USB) mode
1	1	pass-through(USB) with CDP Emulation

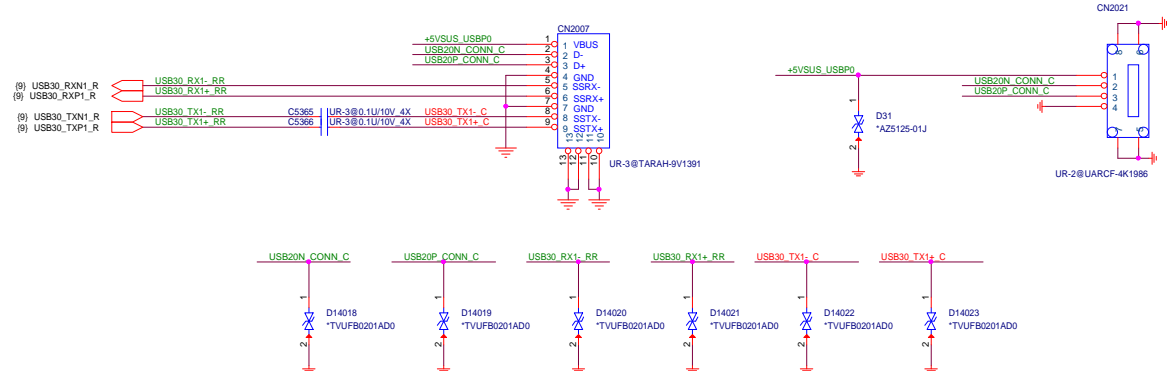
Charger , AM2
Charger , FM
USB , PM
USB , CM

SW3	SW2	14642
CB1	CB0	Status
X	0	2A Auto mode for Apple device
0	1	Pass-Through(USB) mode
1	1	pass-through(USB) with CDP Emulation

Charger , AM2
USB , PM
USB , CM



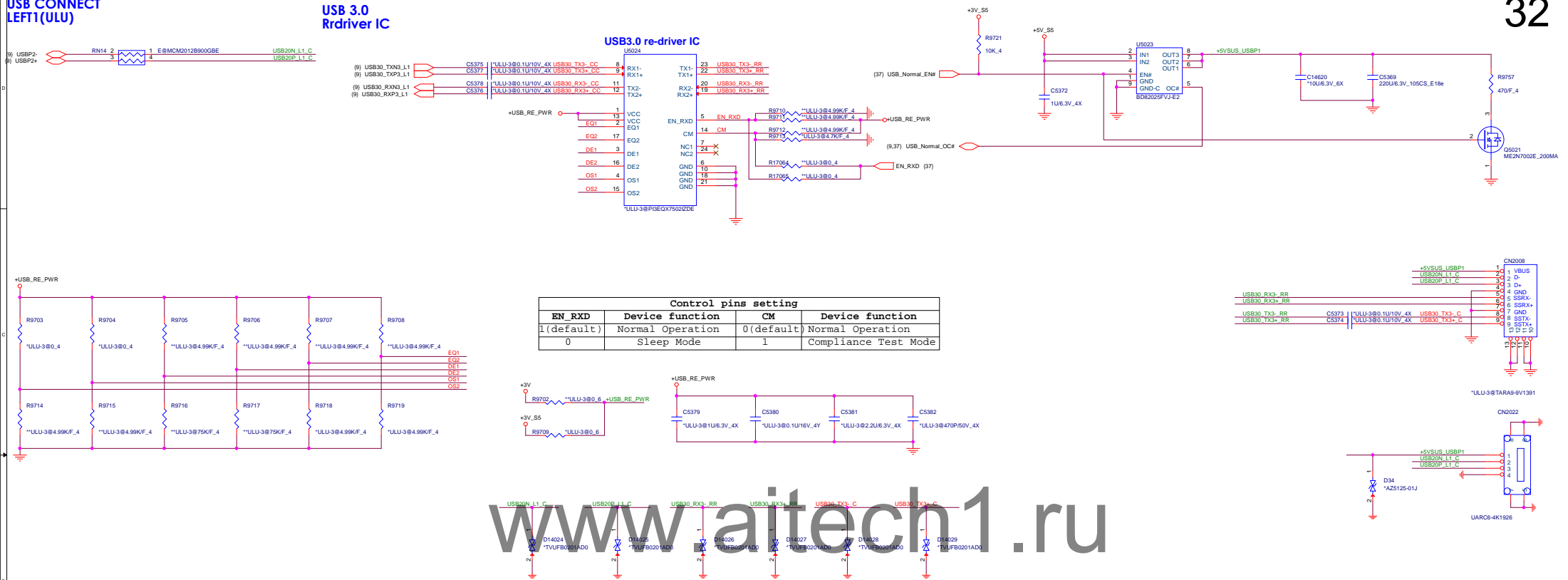
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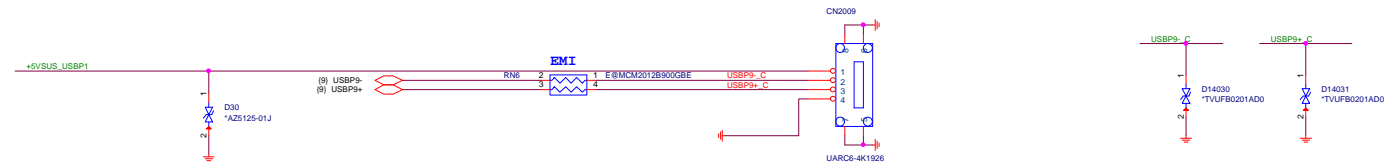
USB CONNECT LEFT1(ULU)

USB 3.0 Rdriver IC

USB3.0 re-driver IC

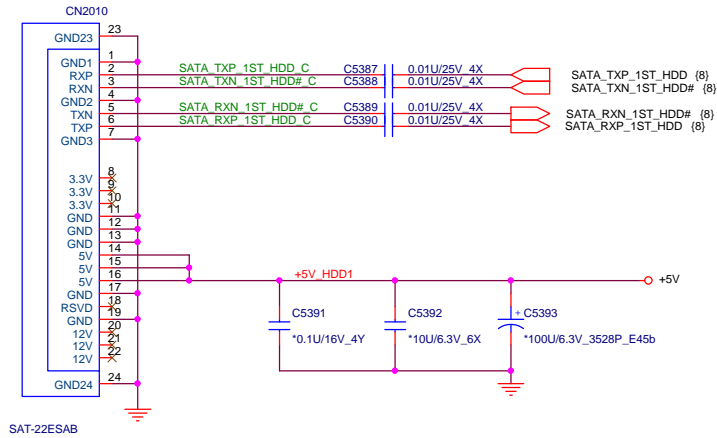


USB CONNECT LEFT2(ULD)



SATA
HDD

HDD

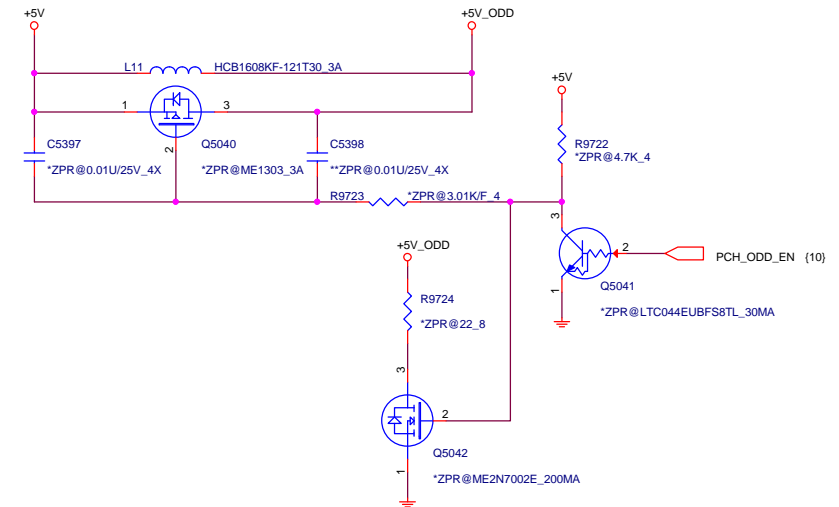
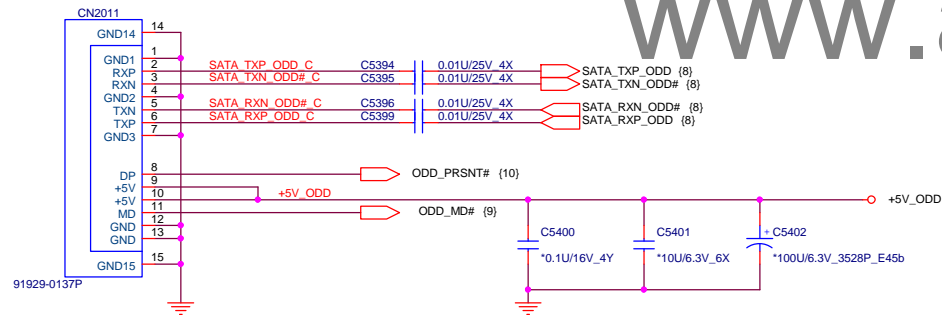


SATA ODD <ODD>

ODD Zero power .
(Only for Intel)

<OZP>

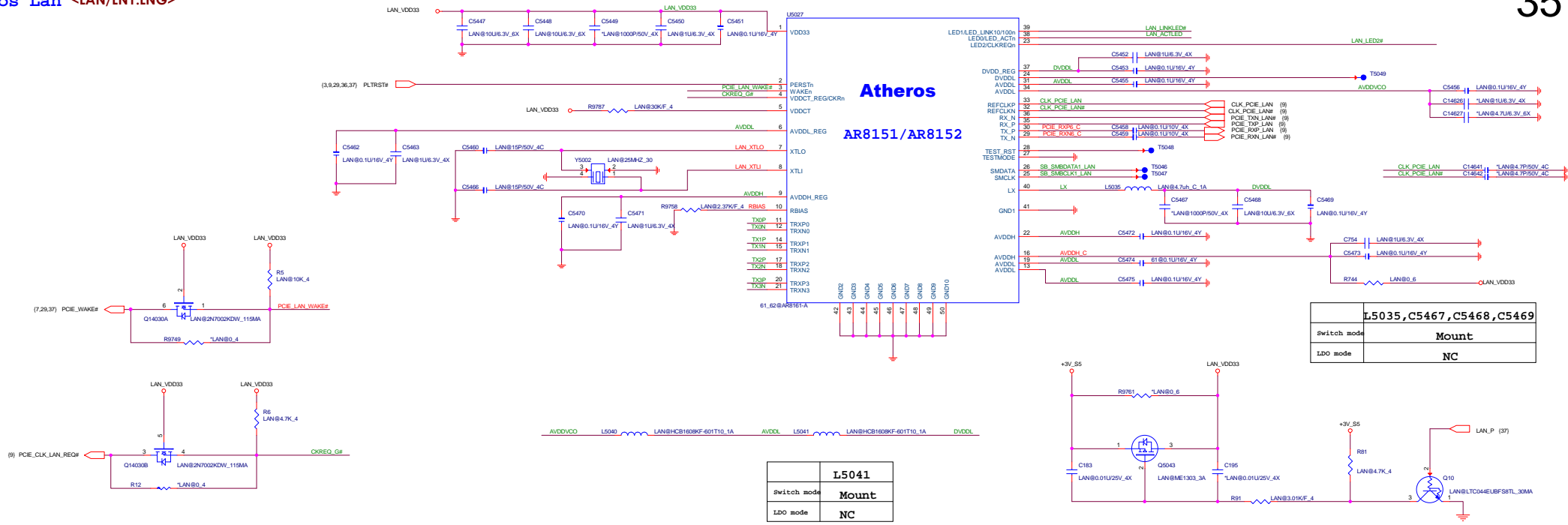
www.aitech1.ru



Atheros Lan <LAN/LN1.LNG>

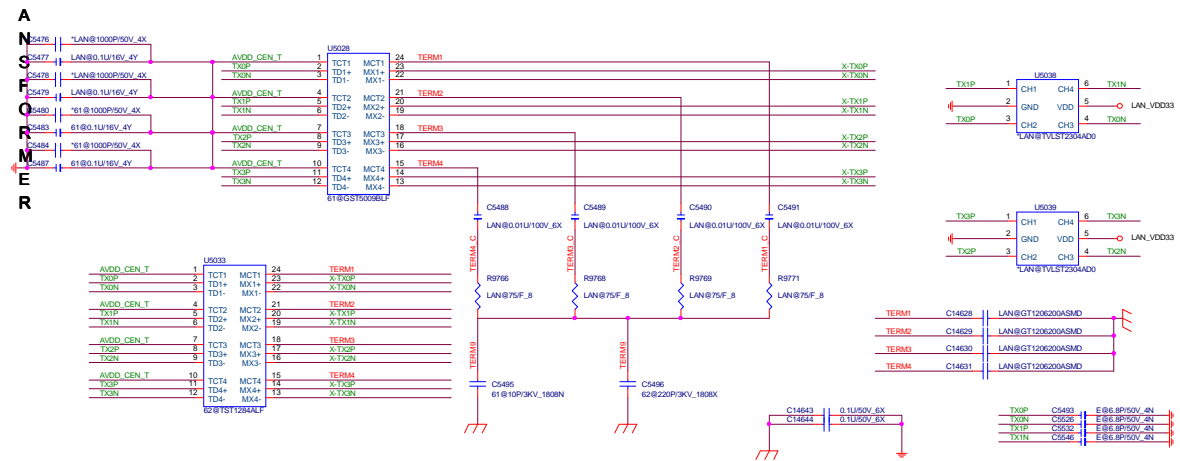
0.163A(20mils)

Atheros
AR8151/AR8152

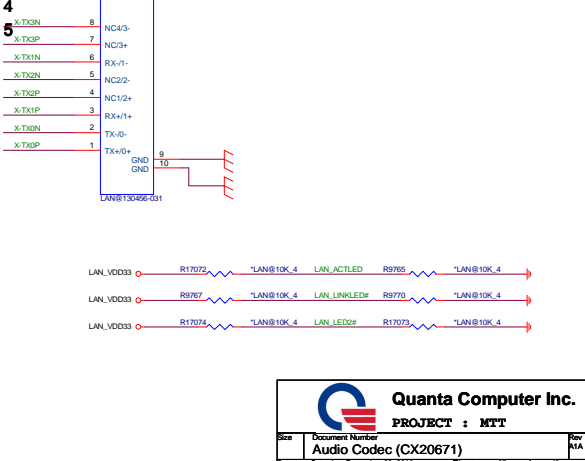


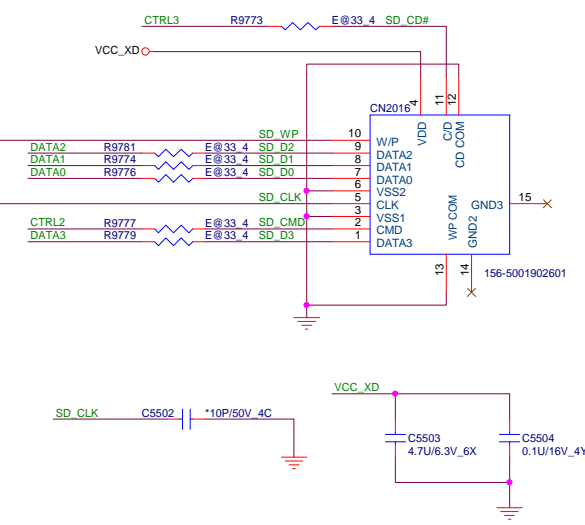
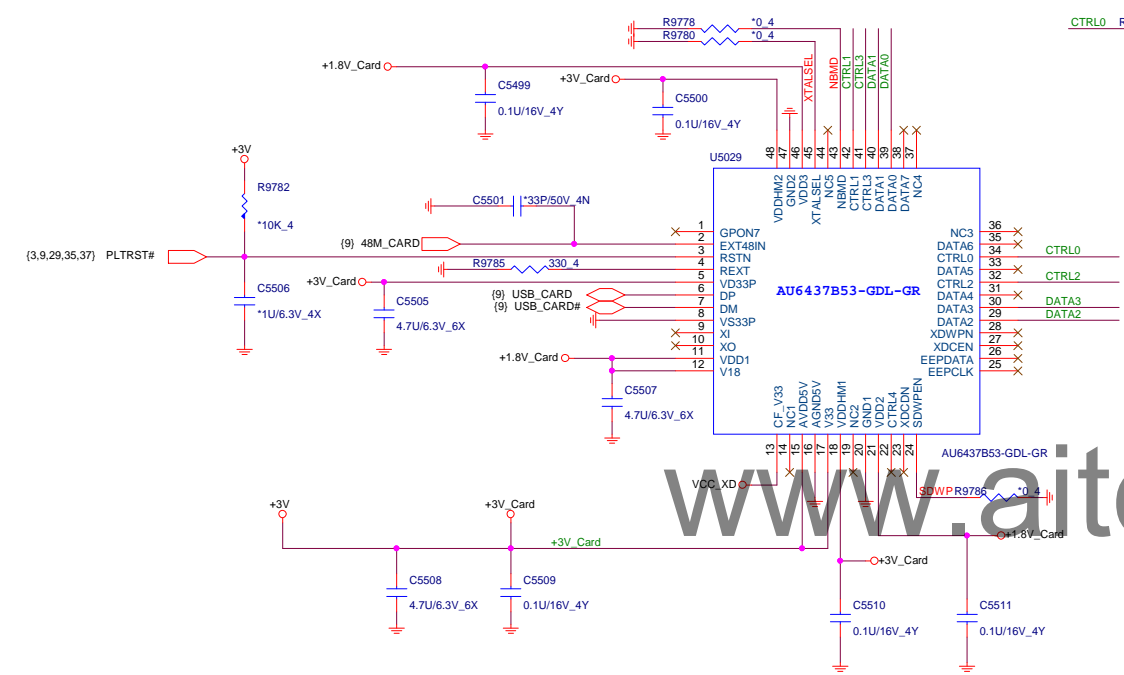
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<LAN/LN1.LNG>




<LAN>





www.aitech1.ru

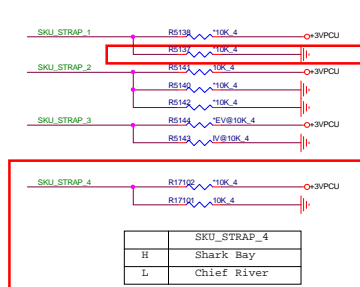
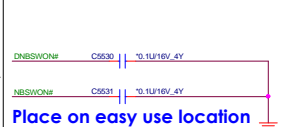
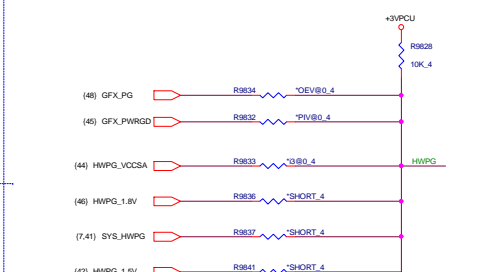
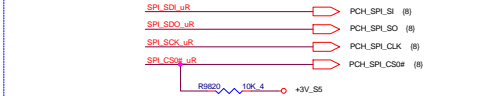
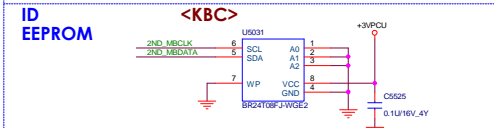
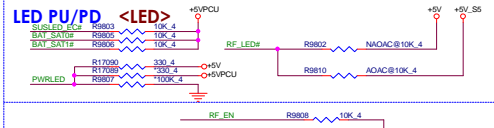
- SDWPEN (SD write protect enable)
1 : decided by SDWP(default)
0 : SD always write-able
- NBMD (Power saving mode enable)
1 : enable (default)
0 : disable
- XTALSEL (Clock input selection)
1 : 48MHz input (default)
0 : 12MHz input

**Quanta Computer Inc.**
PROJECT : MTT

Size	Document Number	Rev
	Card Reader(AU6437)	A1A
Date:	Saturday, December 22, 2012	Sheet 36 of 49

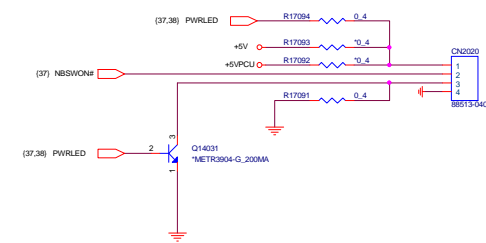
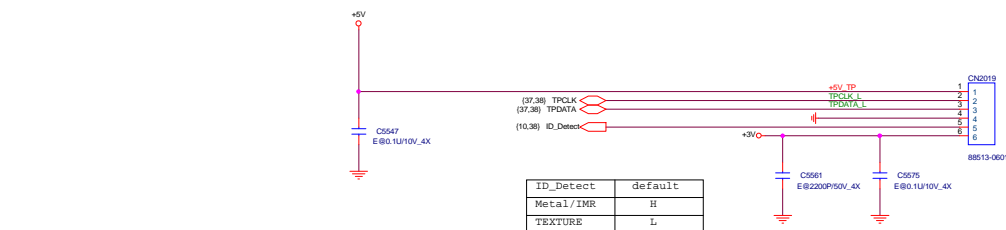


SMBUS	Devices	Address
1	Battery(A)	
2	PCH(S5)	
	G-sensor(S0)	
	CPU Thermal(A)	98H
	IDROM(A)	
3	VGA Thermal(A or S0)	98H
	CEC(A)	
	MMB(A)	



	Capetown@/Luxor@		EV@ / IV@
MS Strap	SKU_STRAP_1	SKU_STRAP_2	SKU_STRAP_3
13" UMA	0	0	0
13" DIS	0	0	1
14" Capetown UMA	0	1	0
14" Capetown DIS	0	1	1
14" Luxor UMA	1	0	0
14" Luxor DIS	1	0	1

TP board <TPD>

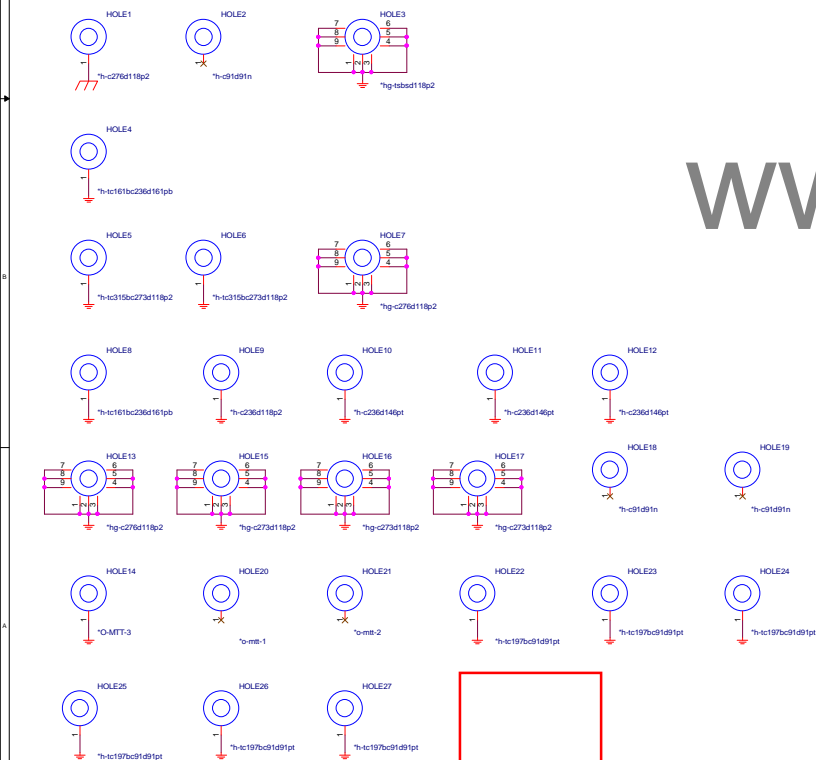


TP board <TPD>



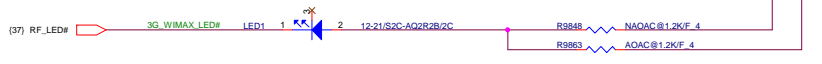
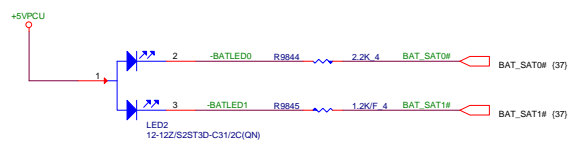
Need add Level Shift on daughter board for 3V/5V TP Device

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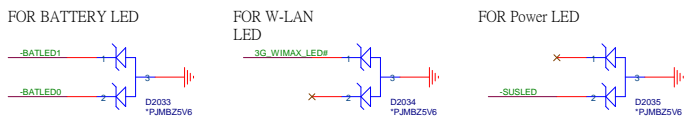
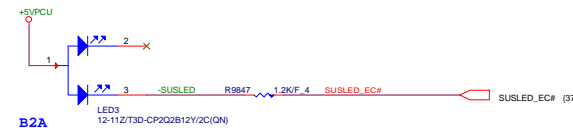
LED BATTERY

RF LED



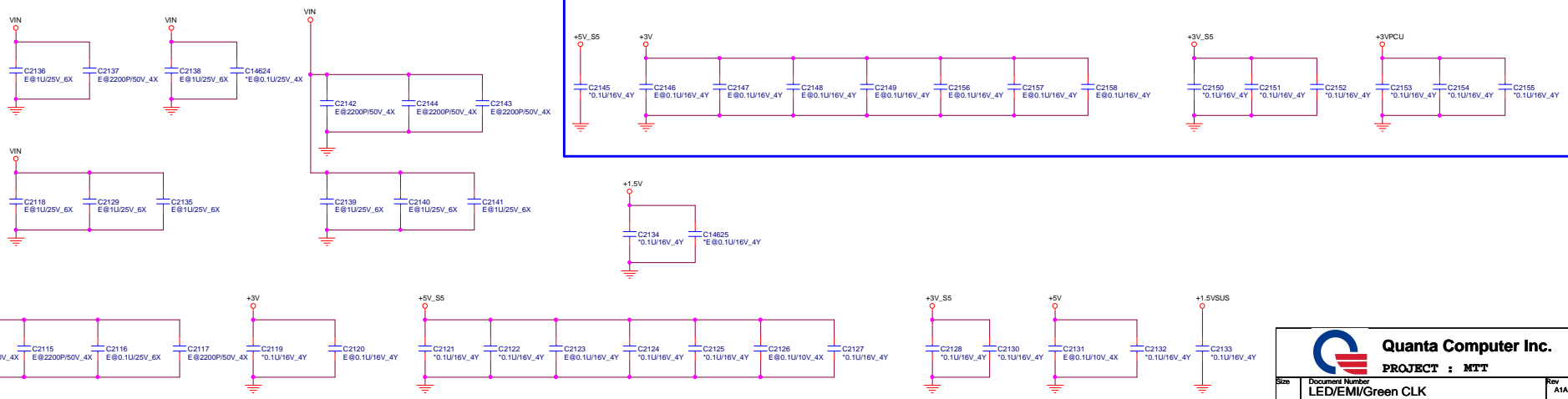
POWER LED

ESD Protect LED

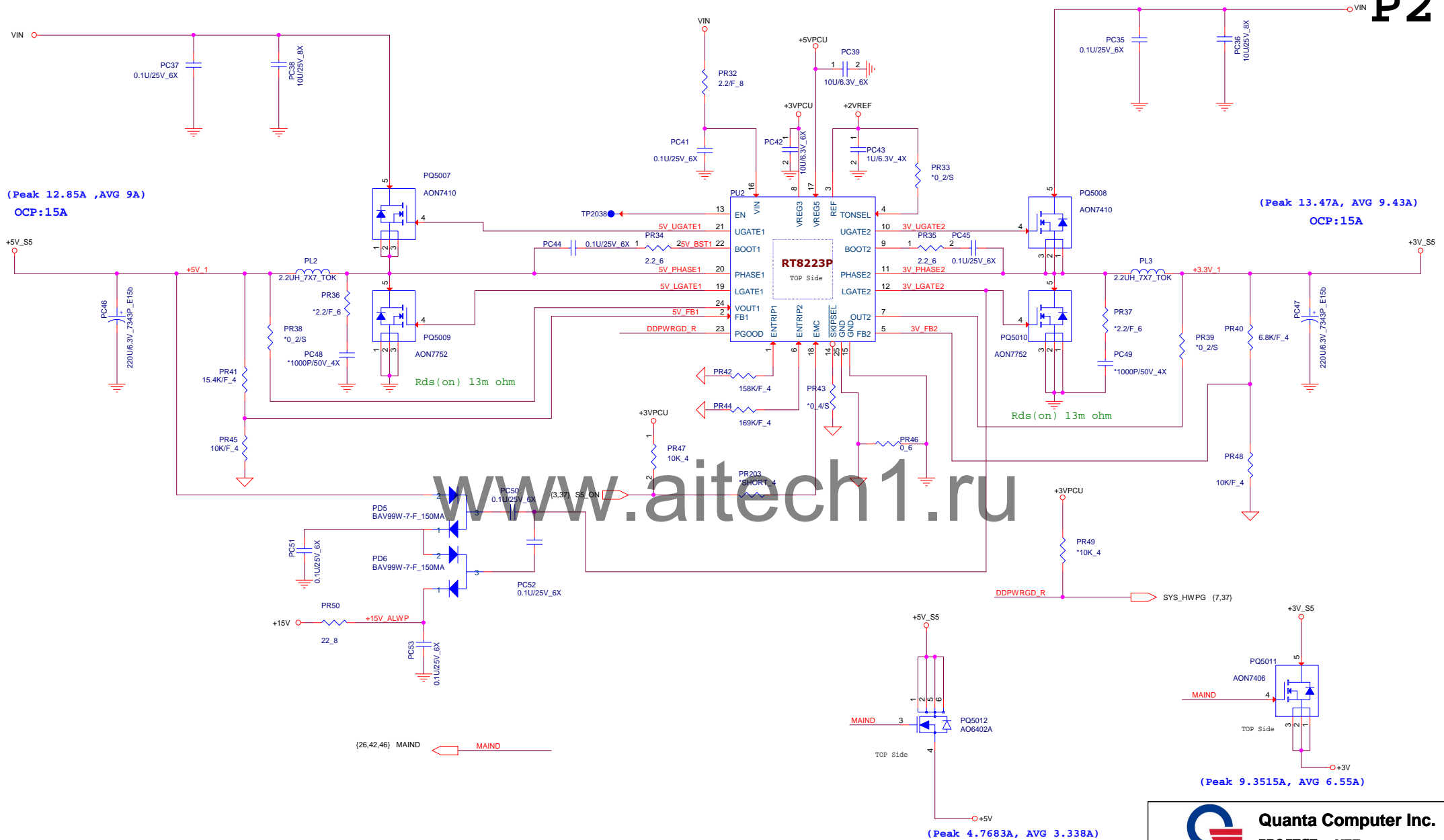


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EMI





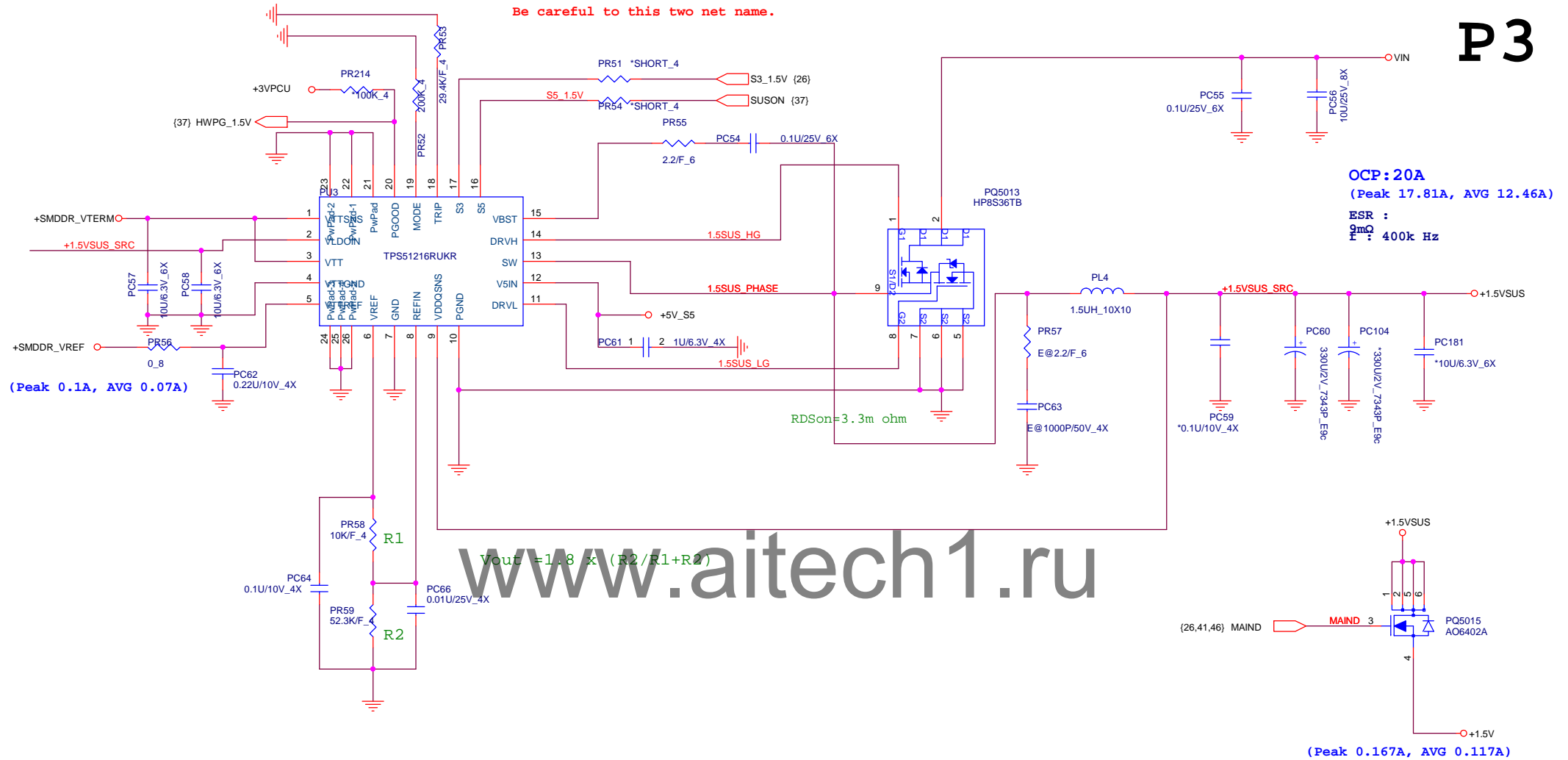


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PROJECT : MTT

Size	Document Number	Rev
	System 3V/5V(TPS51123A)	A1A
Date:	Saturday, December 22, 2012	Sheet 41 of 49

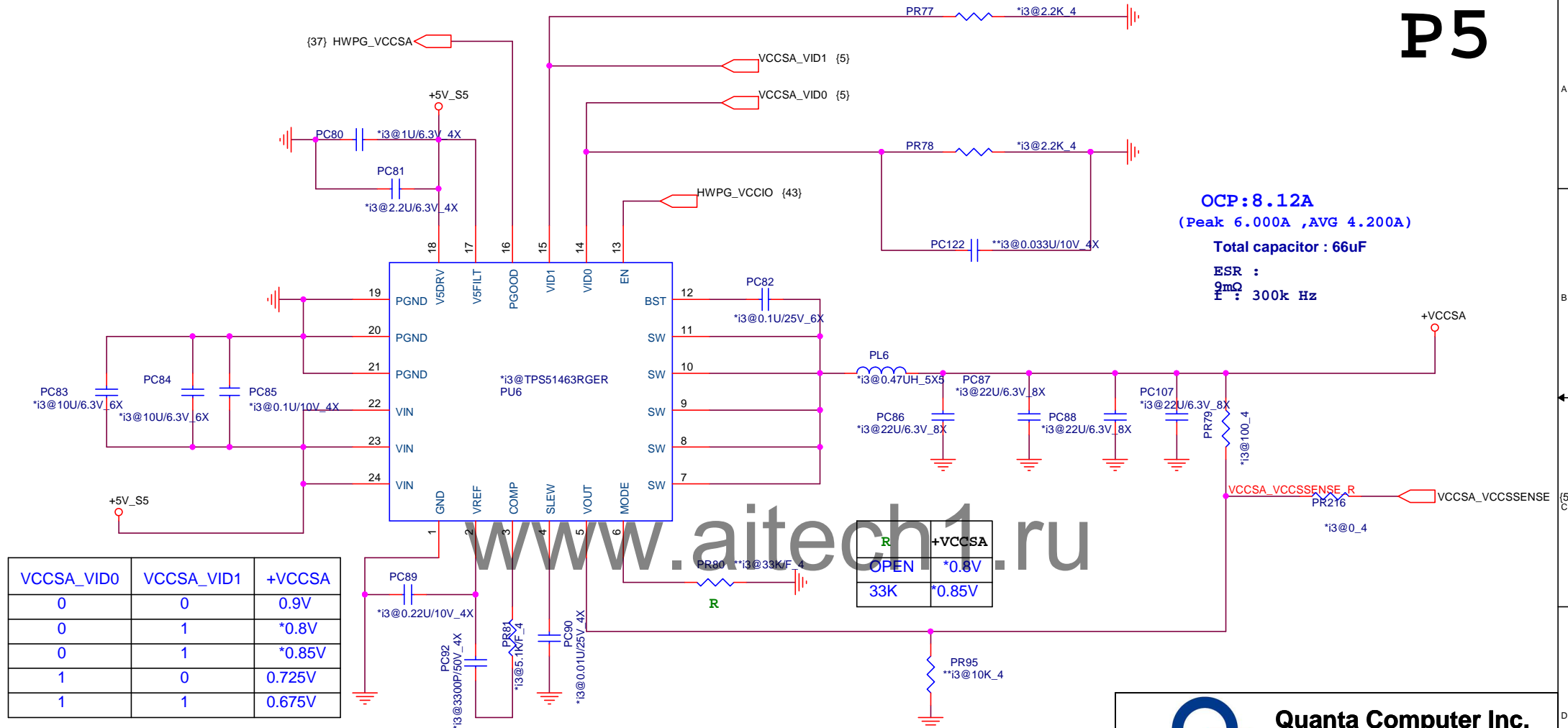
Be careful to this two net name.





$$V_{OUT} = (1 + R_1/R_2) * 0.5$$

Size	Document Number +VCCIO(RT8240BGQW)	Rev A1A
Date:	Saturday, December 22, 2012	Sheet 43 of 49

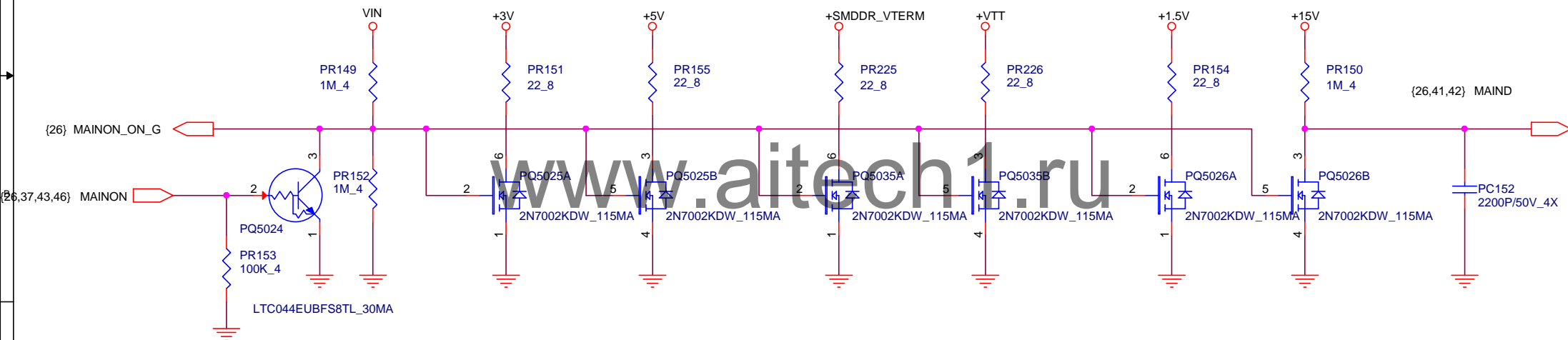
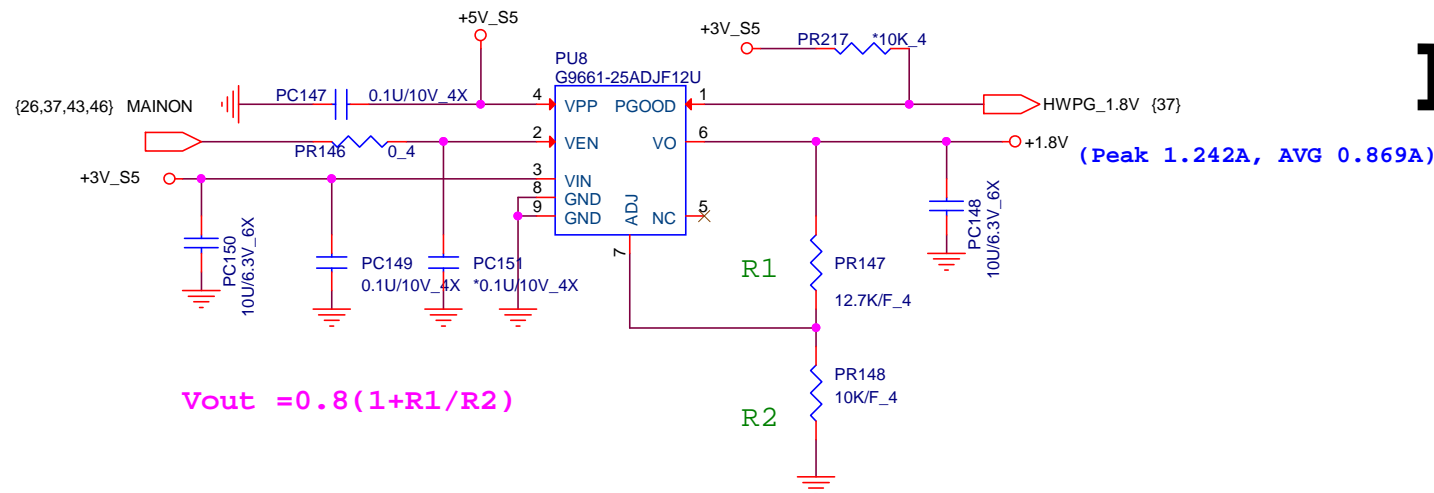



Quanta Computer Inc.
PROJECT : MTT

Size	Document Number	Rev
	+VCCSA(TI51461)	A1A
Date:	Saturday, December 22, 2012	Sheet 44 of 49

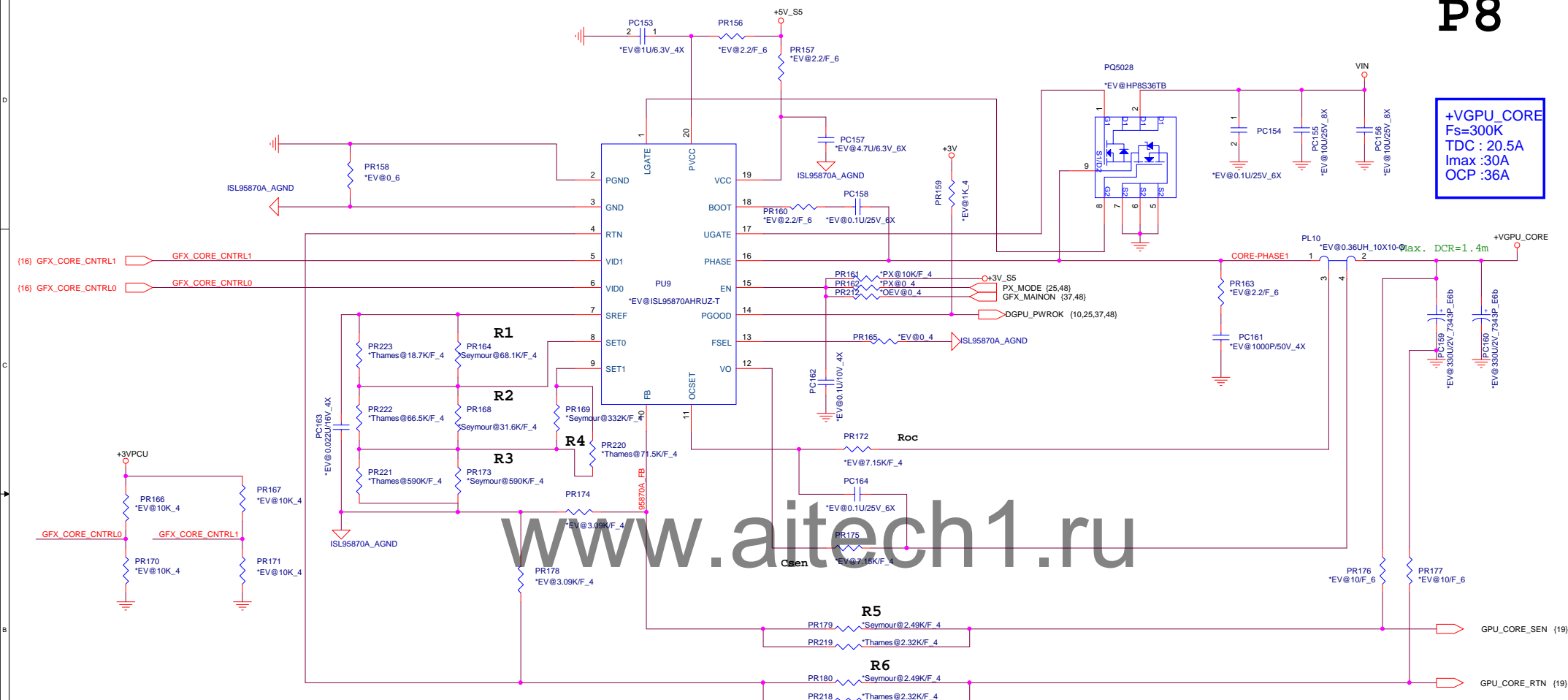


P7



		Quanta Computer Inc.	
		PROJECT : MTT	
Size	Document Number		Rev
	+1.8V/Discharge		A1A
Date:	Saturday, December 22, 2012	Sheet	46 of 49

+VGPU_CORE
 Fs=300K
 TDC : 20.5A
 I_{max} : 30A
 OCP : 36A



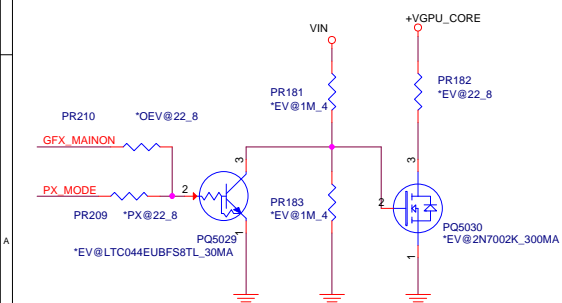
Seymour XT

GFX_CORE_CNTRL1	GFX_CORE_CNTRL0	+VGPU_CORE
1	1	0.9V
1	0	1V
0	1	1.05V
0	0	1.15V

Thames XT

GFX_CORE_CNTRL1	GFX_CORE_CNTRL0	+VGPU_CORE
1	1	0.875V
1	0	0.9V
0	1	1V
0	0	1V

	Seymour XT	Thames XT
R1	68.1K	18.7K
R2	31.6K	66.5K
R3	590K	590K
R4	332K	71.5K
R5	2.49K	2.32K
R6	2.49K	2.32K



Quanta Computer Inc.
 PROJECT : MTT

Size Document Number GPU Core (ISL62881C) Rev A1A
 Date: Saturday, December 22, 2012 Sheet 47 of 49

Model		REV	CHANGE LIST			MODEL		MTT	
MTT	A1A	Schematic Release				PAGE	FROM	To	
	B2A	Page 27:HDMI support Dongle feature with AP2337 HDMI Power switch.				1	1A		
		Page 27:Remove CEC feature , 2013 CEC feature not support.				2	1A		
		Page 35:Change LAN schematic from AR8151/52 to AR8161/62				3	1A		
		Page 43: Reverse PC196 and change PL5 footprint for support Celeron CPU and change PR67 value to 66.5K/F_4				4	1A		
		Page 5: Add R17083/R17084 and change R197 value to add i3@ for support Celeron CPU				5	1A		
		Page 44: Change VCCSA schematic value to add i3@ for option i357 / Celeron CPU				6	1A		
		Page 38: Add MOS to support LED EC pin change from low-active to high-active and change Hole14 Footprint for ME placement				7	1A		
		Page 35: Change CN2015 pin9 and hole1 from LAN_GND to GND				8	1A		
		Page 37: Change R9827 Value from *short0402 to *0_4 for EC985 leaking current issue and change U5030 from 885 to 985				9	1A		
		Page 37: Change R9807 Value to 100K_4 PD and and EC GPIO66(CAP LED) change to GPIO33				10	1A		
		Page 8: R2075 PU from +3V_S5 to +V3A				11	1A		
		Page 10: Add board ID 16/17 for Celeron/i357 CPU				12	1A		
						13	1A		
						14	1A		
						15	1A		
						16	1A		
						17	1A		
						18	1A		
						19	1A		
						20	1A		
					21	1A			
					22	1A			
					23	1A			
					24	1A			
					25	1A			
					26	1A			
					27	1A			
					28	1A			
					29	1A			
					30	1A			
	www.aitech1.ru								
DOC NO. 204	PROJECT MODEL :		MTT	APPROVED BY:		DATE:		Size Document Number PROJECT : MTT Change list Rev 1A	
	PART NUMBER:			DRAWING BY:		REVISION:			

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